DESIGN OF A RECONFIGURABLE LOW-NOISE AMPLIFIER IN A SILICON-GERMANIUM PROCESS FOR RADAR APPLICATIONS

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DESIGN OF A RECONFIGURABLE LOW-NOISE AMPLIFIER IN A SILICON-GERMANIUM PROCESS FOR RADAR APPLICATIONS

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SUMMARY

This work explores the design of a reconfigurable low-noise amplifier (LNA) as part of a larger radar system. Chapter I discusses the motivation for reconfigurable radar design. In addition, it gives a summary of the silicon-germanium technology used in this work and its benefits for RF circuit design. Finally, the chapter concludes with an introduction to noise theory and a basic phased-array radar architecture.

Chapter II highlights the designs of two types of switches. The first switch is a single-pole, single-throw switch which can be used as building block for complex reconfigurable networks. The second switch is a single-pole, double-throw transmit/receive switch which can change modes of operation in a radar system. This work, entitled "An X-band to Ka-band SPDT switch using 200 nm SiGe HBTs," was published in Silicon Monolithic Integrated Circuits in RF Systems (SiRF) 2012 [25].

Chapter III discusses the design work for a reconfigurable LNA. Stability analysis is reviewed in detail and a cutting edge analysis technique is used to provide further insights into amplifier stability. A narrow-band design without reconfigurable networks is presented as a baseline for reconfigurable designs. Several switchable transistor core topologies are investigated as potential building blocks for a reconfigurable design. Finally, the simulation results for a reconfigurable LNA are presented.

In chapter IV briefly describes the design of a deserializer block. This circuit reduces the number of inputs required to control a reconfigurable system and can significantly decrease the complexity of phased-array radar system. Chapter V finishes with some concluding remarks and discusses future work.

CHAPTER I

INTRODUCTION

1.1 Motivation

Today's radar systems are exposed to a variety of dynamic surroundings. Changes in temperature, weather, and spectral environment all have a significant impact on radar performance. In addition, radar systems have become light-weight and mobile, making it even more important to have high performance across all environmental conditions. The US Frequency Allocation Chart in Figure 1.1 shows that the X-Band (8-12 GHz) segment of the electromagnetic spectrum is very crowded [36]. X-Band is a popular frequency range because the small wave length at these frequencies allows for high resolution, but the relatively low atmospheric attenuation enables longer range systems. In this congested X-Band region, receivers can be subjected to high power signals that can damage amplifiers, as well as low power interfering signals.

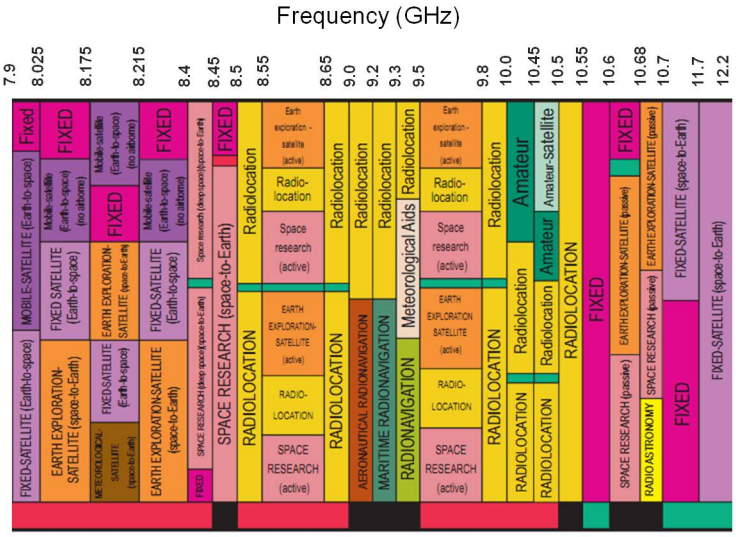

Figure 1.1: X-Band frequency allocation chart [36]

To maintain reliable performance, multiple radar systems may be utilized in combination. For example, aircraft radar typically uses both C-Band (4-8 GHz) and X or Ku-Band (12-18 GHz). The C-Band system is crucial because it is less susceptible to signal degradation caused by rain and fog. The X or Ku-Band radar has better resolution and is used for air-traffic control radar [11]. While having multiple radar systems can help prevent disruptions in a changing environment, it comes at a high cost. Clearly, if a single radar system could reconfigure to its environment, there would be tremendous benefits in terms of size, cost, and reliability. This work investigates the critical building blocks for such a system using Silicon-Germanium (SiGe) Heterojunction Bipolar Transistors (HBTs).

1.2 Silicon-Germanium Heterojunction Bipolar Transistor

For many decades, radio frequency (RF) applications have been dominated by III-V materials such as gallium arsenide (GaAs) and indium phosphide (InP). However, the advances in the silicon (Si) fabrication process have led to significantly reduced fabrication costs on Si. Unfortunately, the device performance required at high frequencies has prevented silicon products from playing a major role in the RF market. The main limitation of the high frequency performance in silicon is its comparatively lower electron and hole mobilities [6].

As early as 1948, William Shockley realized that combining materials of different bandgaps could create beneficial semiconductor devices [31][17]. As silicon began to dominate the semiconductor industry, there was great interest in adding germanium to the silicon base in a Bipolar Junction Transistor (BJT) to improve the transistor performance. However, the challenges of reliably adding germanium into the base without causing lattice defects prevented such devices from being realized. In the mid-1980s, Benard Meyerson developed an ultrahigh-vacuum/chemical vapor deposition (UHV/CVD) low-temperature epitaxy (LTE) technique to deposit a SiGe base

layer within the thermal constraints of the fabrication process [15]. This was a pivotal breakthrough that quickly led to the first functional SiGe HBTs. Since this achievement, the performance of the devices has rapidly improved.

The two main figures of merit used to benchmark high frequency transistor performance are the unity gain cut-off frequency (f_T) and the maximum oscillation frequency (f_{max}). The f_T of the device indicates the frequency where the current gain with a short circuited output becomes unity. The maximum oscillation frequency is the highest frequency at which the matched transistor produces power gain. Figure 1.2 shows the improvement in f_T and f_{max} over generations of SiGe HBTs [40]. SiGe HBTs have now reached an f_T and f_{max} above 300 GHz. In addition, SiGe HBT fabrication is compatible with the typical CMOS processes and only requires a few additional steps. As a result, SiGe offers III-V like performance with the low-cost and high-yield of silicon fabrication. This has allowed SiGe HBTs to become competitive with III-V devices for RF applications.

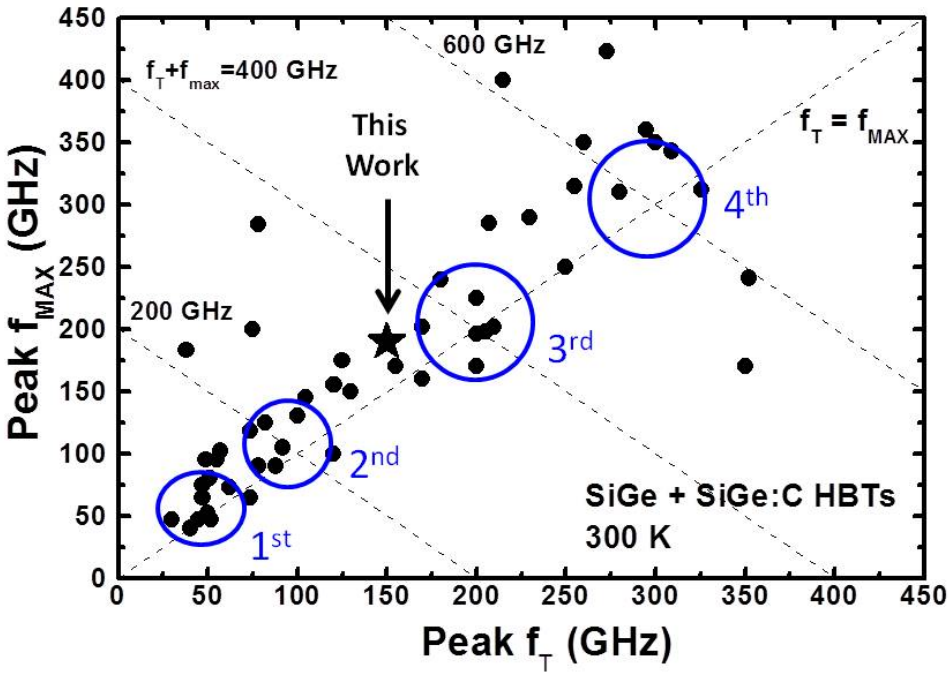

Figure 1.2: SiGe (f_T) and (f_{max}) over generation [40]

The benefits of adding germanium (Ge) to the transistor are at a basic level the result of changing the bandgap. Silicon has a bandgap of 1.12 eV, and germanium has a bandgap of 0.66 eV. For every 10% Ge introduced into the Si lattice, the bandgap decreases about 75 meV [6]. When Ge is deposited into the base of the transistor, the reduction in the bandgap manifests itself as a decrease in the conduction band. By tightly controlling the SiGe epitaxial deposition, the bandgap can be tailored across the transistor base. Typically, the amount of Ge is relatively low at the emitter-base (EB) junction and is increased toward the collector-base (CB) junction as shown in Figure 1.3.

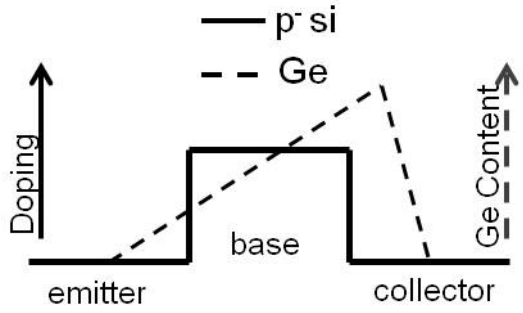

Figure 1.3: Simple germanium grading profile in the transistor base

The increase in germanium content causes the bandgap to decrease over the width of the base and is known as germanium grading. Figure 1.4 shows the energy band diagram of a graded SiGe HBT, where $\Delta E_{g,Ge}(x = 0)$ and $\Delta E_{g,Ge}(x = W_b)$ represent the reduction in the bandgap due to the Ge content at the EB and CB junctions. The change in the bandgap over the base width is defined as $\Delta E_{g,Ge}(Grade) = \Delta E_{g,Ge}(x = W_b) - \Delta E_{g,Ge}(x = 0)$.

Similar to a BJT, if the emitter-base junction is forward biased, the potential barrier at the junction is reduced and electrons easily flow from the emitter to the collector. Holes also flow back from the base to the emitter, but the emitter is doped significantly higher than the base so the collector current is much larger than the base current. This results in a base to collector current gain (β).

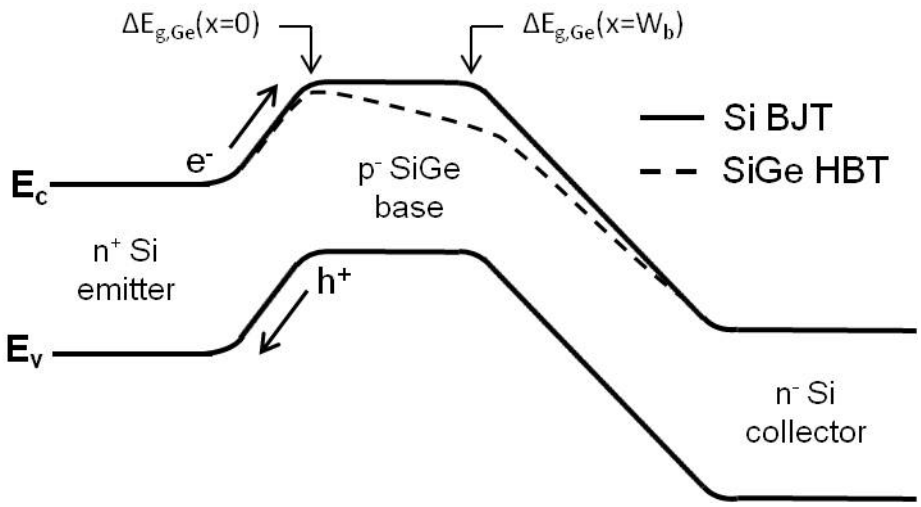

Figure 1.4: SiGe HBT band diagram with Ge graded base [6]

The energy band diagram in Figure 1.4 shows that the germanium content at the emitter-base junction reduces the barrier for electrons in the emitter to jump into the conduction band. This reduction exponentially increases the current gain of the device. In comparison to a Si BJT with a similar structure and feature size, the ratio of the current gain of a SiGe HBT to a Si BJT is given in Equation (1.1),

$$\frac{\beta_{SiGe}}{\beta_{Si}} = \frac{\tilde{\eta}\tilde{\gamma}\Delta E_{g,Ge}(Grade)/(KT) \times e^{\Delta E_{g,Ge}(x=0)/(KT)}}{1 - e^{-\Delta E_{g,Ge}(Grade)/(KT)}}, \tag{1.1}$$

where $\tilde{\gamma}$ is the effective density of states ratio between SiGe and Si, and $\tilde{\eta}$ is the minority electron diffusivity ratio between SiGe and Si [6]. This equation shows that the improvement in current gain of SiGe HBTs is related linearly to the grade of the germanium deposition and related exponentially to the germanium band offset at the emitter-base junction. The increase in current gain provides many benefits for high performance circuit design.

In addition to the benefits in DC current gain, the SiGe HBT also provides AC performance benefits. While the change in bandgap over the base width may only be around 100meV, it occurs over a distance of tens of nanometers. As a result, the grading creates a powerful electric field which accelerates electrons close to their

saturation velocity. This greatly decreases the transit time in the base and increases the transistor speed. Equation (1.2) shows the transit time in the base, τ_b, directly effects the unity gain frequency,

$$f_T = \frac{1}{2\pi\tau_{ec}} = \left[g_m(C_{te} + C_{tc}) + \tau_b + \tau_e + \frac{W_{CB}}{2v_{sat}} + r_c C_{tc} \right]^{-1}, \tag{1.2}$$

where τ_{ec} is the collector-emitter transit time, g_m is the intrinsic transconductance, C_{te} and C_{tc} are the emitter-base and collector-base depletion capacitances, τ_e is the emitter charge storage time, W_{CB} is the width of the collector-base space charge region, v_{sat} is the saturation velocity, and r_c is the dynamic collector resistance [6]. As a result of the field induced by the Ge grading, τ_b is significantly reduced, and SiGe HBTs can operate at much higher frequencies than Si BJTs.

1.3 Transistor Noise

Noise is a fundamental limitation of any communication system. Any environment naturally contains some background noise that can corrupt a weak communication signal. In order for a receiver to accurately process a signal, there must be a significant signal-to-noise ratio (SNR). Unfortunately, the receiver electronics and transistors themselves add noise to the signal and degrade the SNR. As a result, an important goal of any receiver is to minimize the noise added to the system. Figure 1.5 shows the probability of error as a function of the carrier-to-noise ratio for common communications modulation schemes [12]. The plot indicates that a slight decrease in the carrier-to-noise ratio can increase the probability of error by several orders of magnitude.

The inherent properties of SiGe HBTs enable low noise design. The main high frequencies noise sources in a bipolar transistor are the shot noise in the emitter-base and collector-base junctions, and the thermal noise associated with the base spreading resistance. Shot noise occurs at pn junctions when particles randomly

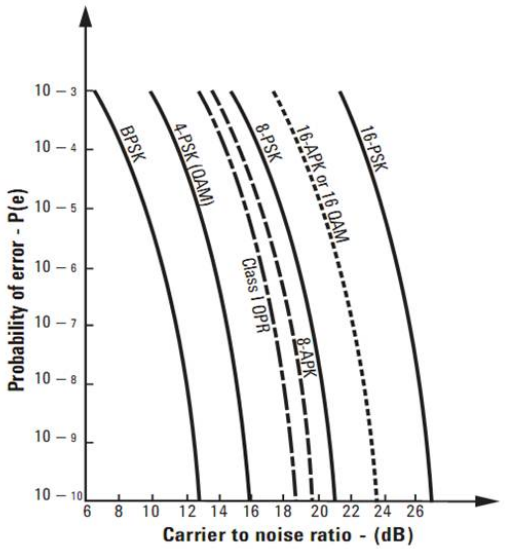

Figure 1.5: Probability of error vs. carrier-to-noise ratio for different modulation schemes [12]

exceed the barrier necessary for DC current flow. As seen in Equations (1.3) and (1.4), the shot noise at a junction is proportional to the DC current through the junction. In these equations, i^2_{shb} is the shot noise current at the base; i^2_{shc} is the shot noise current at the collector; I_b and I_c are the DC base and collector currents; q is the charge of an electron, 1.602 x 10-19 C, and Δf is the system noise bandwidth [20]. The thermal noise associated with the base spreading resistance is used to represent the two dimensional flow of current across the emitter-base junction. This effect can be modeled to first order using Nyquist's formula shown in Equation (1.5), where K is Boltzmann's constant (1.38x10-23 J/K) [6].

$$i^2_{shb} = 2qI_B\Delta f \tag{1.3}$$

$$i^2_{shc} = 2qI_C\Delta f \tag{1.4}$$

$$v_t^2 = 4KTR_b\Delta f \tag{1.5}$$

These sources can be added externally to the HBT model to approximate the effects of noise on the circuit. Figure 1.6 shows the SiGe HBT model including the noise sources. The direction of the sources is arbitrary since i_{shb}^2 and i_{shc}^2 are root means squared averages and the current may vary in either direction. The shot noise at the base has a much larger impact than the shot noise at the collector because the noise at the base is amplified by the gain of the transistor.

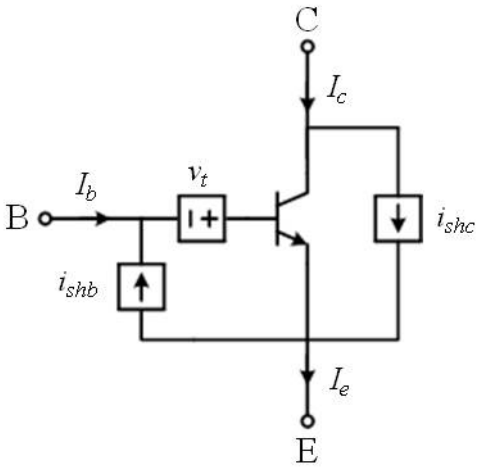

Figure 1.6: SiGe HBT noise model

Using the model shown in Figure 1.6 and assuming that $g_m r_b >> \frac{1}{2}$, the minimum noise factor can be estimated by Equation (1.6). This equation highlights the benefits of using SiGe HBTs for low noise design. The SiGe enhancements in β and f_T described earlier both reduce the noise of the transistor [23].

$$F_{min} = 1 + \frac{1}{\beta} + \sqrt{2g_m r_b}\sqrt{\frac{1}{\beta} + \left(\frac{f}{f_T}\right)^2} \tag{1.6}$$

1.4 Phased-Array Radar

Radar was initially developed during World War II as an early detection system for aircraft and antiaircraft weapons. Today, it is used in a variety of applications

including air traffic control, security scanners, collision prevention for cars, and meteorology. Radar systems transmit a high frequency signal that propagates through the atmosphere and reflects back when it hits an object. The distance of the object can be calculated from the time it takes the signal to travel to the object and return [32].

Early radar systems scanned in different directions by mechanically steering radar dishes. Today, phased-array radar offers further flexibility using many separate signals with small phase shifts to enable electronic beam steering. Digital controls adjust the phase shifts so the signals added constructively or destructively to create the desired beam pattern. A block diagram of a simple phased-array radar system is shown in Figure 1.7. The diagram shows that each antenna element has the same supporting electronics called transmit and receive modules (TRM).

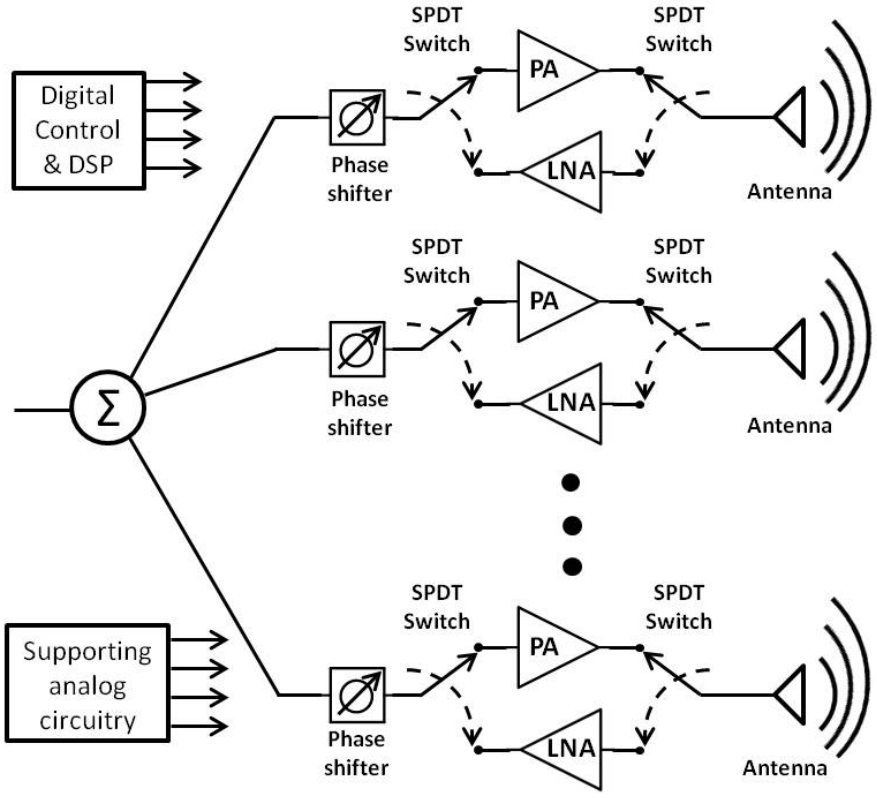

Figure 1.7: Simple phased-array block diagram

Each TRM includes a path for both receiving and transmitting signals, which is selected by switches. In the receive path, an RF signal comes in through the antenna, to the first single-pole, double-throw (SPDT) switch. Both SPDT switches are connected to the LNA in receive mode. The low power signal received by the antenna passes through the switch and is amplified by the LNA. The phase shifters constructively or destructively combine the signals in each TRM. The combined signal is then down converted to baseband. In the baseband, analog-to-digital converters (ADC) transfer the signal into the digital domain where digital signal processing can extract the distance, speed, and direction of an object [9]. SiGe is a cost effective platform for phased-array radar because it can integrate the RF, analog, and digital electronics at a low cost. This allows for a large number of TRMs to be integrated into a single system.

In the transmit path, a waveform generator creates the initial signal, which is split to many TRMs. The signal is shifted in each TRM to create the desired beam pattern and is then passed through the switch to the power amplifier. The power amplifier significantly increases the power of the signal so that it can be detected over long distances.

The LNA is an extremely important block in the receive path. The purpose of the LNA is to amplify the weak signal coming in from the antenna while adding as little noise to the signal as possible. Low noise is critical for circuits early in the receiver chain because any noise they add to the system is amplified by all subsequent blocks. The noise factor of a system can be related to the noise factor and gain of individual blocks by Friis' Equation (1.7) [10]. The noise factor translates to noise figure (in dB) through Equation (1.8). Friis' equation highlights that the noise factor of the first stage adds directly into the system noise factor, whereas the noise factor of subsequent stages are reduced by the gain of first stage. In this way, the performance of the LNA essentially dictates the noise figure of the entire system. Clearly to develop a system

with a low noise figure, it is crucial for the LNA to have both a low noise figure and a high gain.

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots + \frac{F_n - 1}{G_1 G_2 \cdots G_n} \tag{1.7}$$

$$NF = 10log(F) \tag{1.8}$$

This work focuses on the design of a reconfigurable LNA and some of the supporting building blocks important in a phased-array radar system. Chapter II focuses on the designs of two different types of switches. The first is a simple switch to change in and out reconfigurable networks. The second design targets a wide band switch to change between transmit and receive paths. Chapter III focuses on the core LNA design. This chapter highlights the stability analysis of an LNA, the design of a baseline LNA, a comparison of reconfigurable transistor core architectures, and the design of a reconfigurable LNA. Chapter IV briefly describes a deserializer design, which enables easy management of digital control signals. Finally, chapter V draws conclusions and discusses future work.

CHAPTER II

SWITCHES

2.1 Single-Pole, Single-Throw

In a reconfigurable design, having small high performance switches enables a large amount of flexibility. Figure 2.1 illustrates some of the possible ways that a switch can be used in the design of a reconfigurable LNA. An RF switch can be used to change the input matching network. This change can shift the frequency of operation, tune to a better power match, or tune to a better noise match. Switches may also be used to switch in additional transistor cores. This can increase output power, avoid saturation, or improve linearity. In addition, using switchable output matching networks can also provide a control knob to alter performance. The wide range of possibilities created by a high performance switch makes it an important building block in this design.

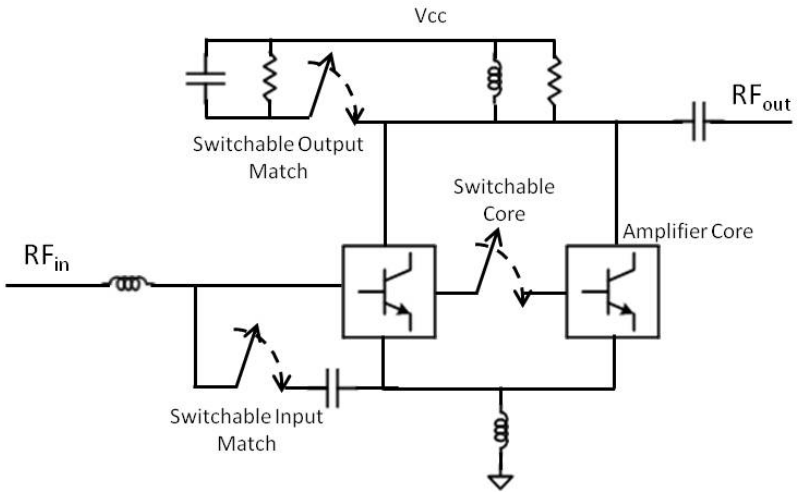

Figure 2.1: Reconfigurable amplifier with switches.

The key design requirements for the switch block are a low insertion loss and high isolation. Insertion loss is the loss over the switch when it is turned on. It is important to minimize insertion loss because any losses added by the switch can have a severe impact on the noise figure of the LNA. The isolation is the ratio of the power at the input to the power at the output when the switch is turned off. Ideally, no power would make it to the output when the switch is turned off, but finite output resistances and leakage paths through the substrate limit the isolation of a switch. Additionally, the switch must be able to handle the power flowing through it without saturating. Usually this is not a limiting factor when the switch is used within an LNA design where the power level is relatively low.

When using switches within an LNA design, it is also important to keep the design as simple as possible to reduce size. The smaller the layout of the switch, the easier it is to add to an LNA. As switches become larger in size, they require more routing, spread the circuit out, and cause additional losses associated with longer transmission lines. In this design, a simple series-shunt topology shown in Figure 2.2 is used to minimize such losses. The MOSFET solution provides good insertion loss, consumes almost no power, and can be seamlessly integrated with the high performance HBTs used in the LNA.

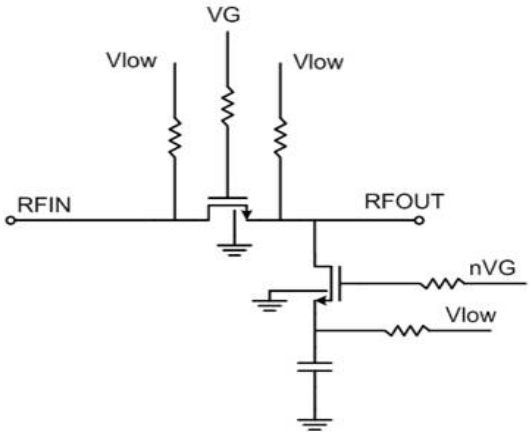

Figure 2.2: Series-shunt SPST topology.

In the schematic diagram, V_{low} provides a DC bias to the source and drain of the nFETs. To turn on the switch, a high voltage is applied to the gate of the series device and a low voltage is applied to the shunt device. The series device allows the RF signal to easily pass through it to the output, while the shunt device presents a large impedance between the output and ground. In the off state, the series device is turned off, and the shunt device is turned on. This prevents the RF signal from reaching the output and shunts any signal leaking through the series device to ground.

To achieve low insertion loss, the impedance across the nFET in the on state must be as small as possible. For nFETs, the lowest impedance occurs when the transistor is biased in the triode region and the slope of the I-V curve is the steepest. Equation (2.1) shows the current equation for an nFET in the triode region. To determine the small signal impedance, the derivative in Equation (2.2) is used. From Equation (2.3), it is clear that the smallest gate length should be used to minimize insertion loss. For this process the minimum gate length is 200 nm. In addition, the gate voltage should be as large as possible, while the bias voltages at the drain and source should be same ($V_{ds} = 0V$). Equation (2.3) also indicates that the gate width should be made as large as possible. This is deceiving though because as the gate width increases, it adds parasitic capacitance that creates more loss at high frequencies. The selection of the gate width must be investigated in further detail.

$$I_d = \frac{\mu_n C_{ox} W}{L} \left[(V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right] \tag{2.1}$$

$$\frac{1}{R_{ON}} = \frac{\partial I_{ds}}{\partial V_{ds}} = \frac{\mu_n C_{ox} W}{L} (V_{gs} - V_t - V_{ds}) \tag{2.2}$$

$$R_{ON} = \frac{L}{\mu_n C_{ox} W (V_{gs} - V_t - V_{ds})} \tag{2.3}$$

To optimize the size of the width of the series and shunt devices, the insertion loss and isolation contours were plotted for a wide range of gate widths at 10 GHz. Figure 2.3 shows the contours of insertion loss and isolation for devices sized between 25 μm and 250 μm. The plot shows that as the gate width of the series device is increased, the insertion loss decreases until the parasitic capacitance associated with the larger device begins to degrade the insertion loss. As a result, there is an optimum width which occurs around 80-100 μm. In this design an 80 μm series device and 60 μm shunt device were selected to achieve both a good insertion loss and isolation.

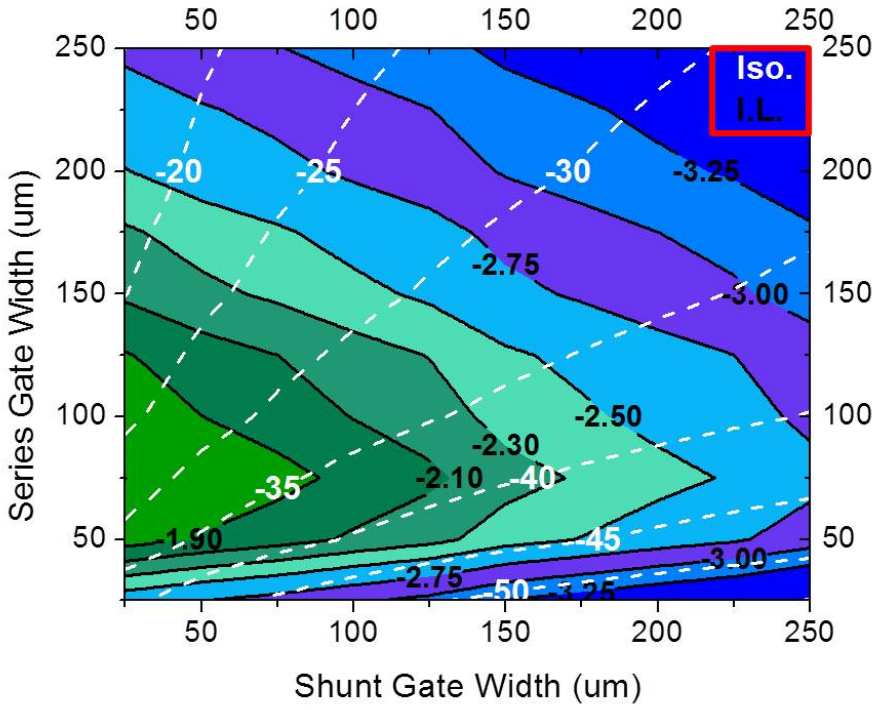

Figure 2.3: Insertion loss and isolation contours at 10 GHz.

On SiGe platforms, the p-type bulk substrate typically has a resistivity on the order of 5-20 Ω-cm [5]. As a result of the relatively low substrate resistivity, the drain-bulk and source-bulk capacitances play a major role in the overall loss of the switch. It has been shown that the losses coupling through the drain-bulk and source-bulk capacitances can be reduced by having a very large substrate resistance or a

very small substrate resistance. Equation (2.4) gives the estimated insertion loss for a single MOSFET [16],

$$IL = \frac{1}{|S_{21}|} = \frac{(R_{ON} + 2Z_0)^2 + \omega^2 C_T^2 \left[(R_{ON} + 2Z_0)\, R_B + (R_{ON} + Z_0)\, Z_0\right]^2}{(2Z_0)^2 \left(1 + \omega^2 C_T^2 R_B^2\right)} \tag{2.4}$$

$$C_T = C_{DB} + C_{SB} + \frac{(C_{GD} + C_{GS})\, C_{GB}}{C_{GD} + C_{GS} + C_{GB}} \tag{2.5}$$

where R_{ON} is the low frequency resistance of the MOSFET, Z_0 is the characteristic impedance of the S-parameter ports, C_T is the equivalent capacitance, and R_B is the substrate resistance. When R_B is very large, there is no loss path through the substrate and Equation (2.4) reduces to Equation (2.6). On the other hand, if R_B is very small, the insertion loss is also decreased and can be simplified to Equation (2.7).

$$IL \approx \left(\frac{R_{ON} + 2Z_0}{2Z_0}\right)^2 \tag{2.6}$$

$$IL \approx \frac{(R_{ON} + 2Z_0)^2 + \omega^2 C_T^2 \left[(R_{ON} + Z_0)\, Z_0\right]^2}{(2Z_0)^2} \tag{2.7}$$

Comparing Equations (2.6) and (2.7), the minimum insertion loss occurs when the substrate resistance is very large. However, often for an integrated circuit design it is impractical to achieve high substrate resistance because other nearby circuits may require substrate contacts. These contacts provide a low impedance path to the conductive substrate. In this work, three switch variations were created to compare the tradeoffs associated with the substrate resistance. The low substrate resistance test structure includes substrate contacts right next to the nFET. The high substrate resistance variant only contained substrate contacts in the pads and the

metal-insulator-metal (MiM) blocking capacitor, over 50 μm away from the nFETs. Figure 2.4 shows a photomicrograph of the SPST test structure. The circuit area without pads is only 70 μm x 100 μm.

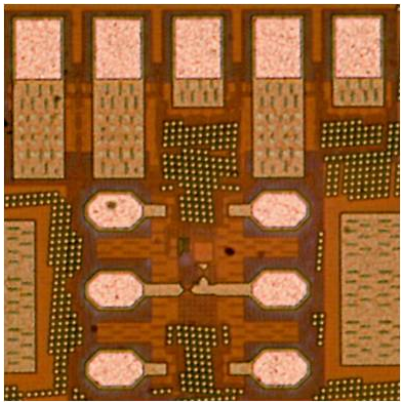

Figure 2.4: Photomicrograph of the SPST test structure.

A more complex switch was also designed in which the substrate resistance could be controlled by an additional nFET, as seen in Figure 2.5. In this design, when the switch is in the on-state, the substrate switch is turned off. In this case, the test structure behaves similar to the high substrate resistance variant and the higher impedance to the substrate limits the leakage paths. When the switch is in the off-state, the substrate switch is turned on allowing the signal to more easily leak through the substrate to ground. This prevents the signal from reaching the output and increases isolation.

The S-parameters of the switch structures were measured using an Agilent E8363B Vector Network Analyzer (VNA) from 1-20 GHz with co-planar ground-signal-ground (GSG) probes. Figure 2.6 shows the measured insertion loss and isolation. As expected, the high substrate resistance switch has the best insertion loss. However, the high substrate resistance also decreases the leakage path through the substrate in the off state and reduces isolation. The design with the extra nFET shows that it in comparison to the low substrate resistance design, it helps prevent leakage through the substrate and improves the insertion loss. In the off state, turning on the substrate

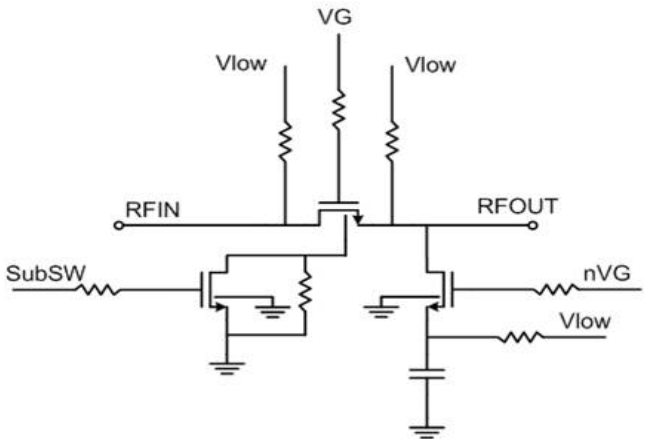

Figure 2.5: Schematic of the SPST with additional substrate switch.

switch increases the leakage through the substrate and improves the isolation in comparison to the high substrate resistance design. Thus, the SPST with the substrate switch provides a good balance of insertion loss and isolation.

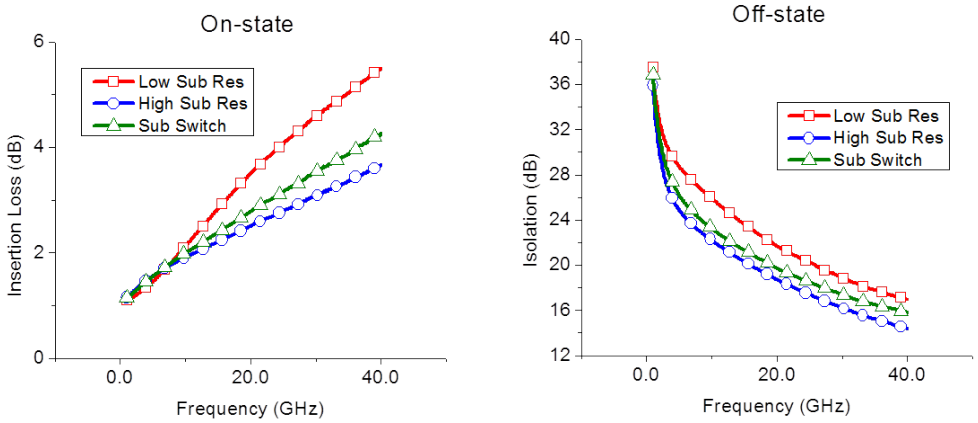

Figure 2.6: SPST measured insertion loss and isolation.

Future work will improve these switches by using resistors and capacitors over an Nwells to increase the isolation to the p^- substrate. Triple well devices will also be explored for improved isolation, but this comes at the cost of increased area and fabrication steps. These switches can easily be extended as building blocks into multi-throw switches. The performance of these small switches is encouraging for applications that switch in and out reconfigurable networks.

2.2 Single-Pole, Double-Throw Transmit and Receive Switch [25]

Single-pole, double-throw transmit and receive (T/R) switches are another key element to a phased-array radar system. The simple phased-array radar architecture seen in Figure 1.7, shows that in order to share the antenna between the transmit and receive paths, a switch is place at the front end of the receiver. The requirements on such switches are extremely demanding. When connected to the receive path the insertion loss of the switch adds directly into the noise figure of the overall receive chain. On the transmit side, the switch must be able to handle the high output power generated by the power amplifier. In addition, the isolation between the transmit and receive paths must be high in order to prevent one path from corrupting the other. Furthermore, when a T/R switch is used in a reconfigurable system, it also needs to be wideband to support different operating frequencies.

2.2.1 Device Comparison

Several different devices are commonly used as T/R switches. Microelectromechanical systems (MEMS) have been designed for switch applications with very low insertion loss and high bandwidth [14]. However, they require a high actuation voltage and are difficult to integrate. CMOS switches offer an extremely low-power solution, but they have a limited bandwidth. PIN diodes can also create switches with good bandwidth and insertion loss, but they consume more power [35]. Table 2.1 displays some of the basic tradeoffs associated with T/R switch design [30]. A fourth option to explore on SiGe platforms is the diode-connected SiGe HBT. When used in a switch configuration, the diode-connected HBT offers a broadband solution that is easy to integrate and has reasonable insertion loss.

Table 2.1: Switch device comparison.

Parameter	*RF MEMS*	*FET*	*Diode*
Bandwith	Large	Small	Large
Insertion Loss	Low	High	Medium
Switching Speed	Slow	Fast	Fast
Power Handling	High	Low	Low
Power Consumption	No	No	Yes
Operating Life	Medium	High	High

2.2.2 Diode-Connected SiGe HBT

A diode can easily be used as a basic switch component. At zero bias, the p-doped and n-doped regions diffuse to create a large space charge region (SCR). The SCR makes it difficult for the signal to pass through the diode. When forward biased, the depletion region shrinks and charge is allowed to flow [24]. At RF frequencies, the forward biased diode presents a very small RF impedance. The SiGe HBT has two junction diodes; the collector-base junction and the emitter-base junction. The collector-base junction has higher parasitic resistances and capacitances due to higher doping, so the emitter-base junction was chosen for the diodes in this work.

Figure 2.7 shows the schematic of the diode-connected SiGe HBT. When V_{in} is set to a high voltage, DC current flows through the RF chokes and turns the diode on, as shown in red. The low impedance in the on state reduces the insertion loss from the input to output, shown in blue. When V_{in} is set to zero, the diode presents a large impedance and prevents the RF signal from flowing from input to output. This leads to high isolation in the off state.

2.2.3 Device Sizing and Biasing

The insertion loss over a diode is determined by its small signal impedance. For an ideal switch, the diode would have zero impedance when turned on and infinite

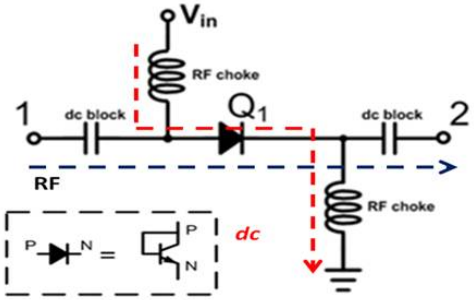

Figure 2.7: Diode-connected HBT test structure.

impedance when turned off. The on state impedance of a diode-connected HBT can easily be found from the pi-network small signal diagram and is given in Equation (2.8) [29]:

$$Z_D = \frac{1}{j\omega\left(C_\pi + C_s\right) + \frac{\beta+1}{r_\pi}} \tag{2.8}$$

This equation indicates that diode impedance, and in turn insertion loss, can be reduced by decreasing r_π. r_π can be decreased with a larger emitter length [6]. Figure 2.8 shows increasing the device length reduces the insertion loss and increases the return loss as desired. The diode configuration also shows extremely wideband characteristics and can be optimized over an 8-40 GHz range.

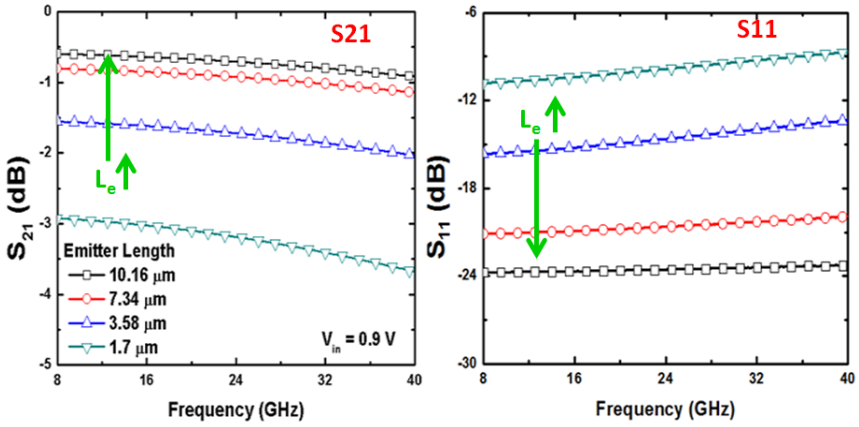

Figure 2.8: S-parameter simulation for different emitter length devices.

The bias voltage also has a large impact on performance because it sets the operating point at which the small signal parameters are extracted. In Figure 2.9, the insertion loss of the diode is plotted for several different bias voltages. The plot on the right shows the change in insertion loss at 24 GHz as a function of the bias voltage. The optimum bias point for minimum insertion loss is at 0.95 V. However, the insertion loss at 0.9 V is still quite good and it requires far less power.

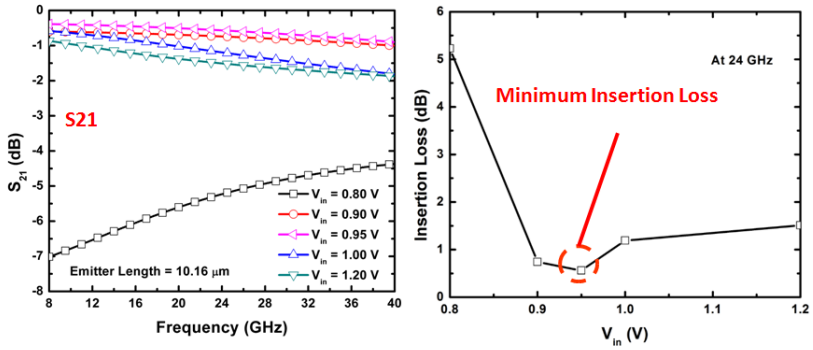

Figure 2.9: Insertion loss simulation for different bias voltages.

2.2.4 Single-Pole, Double-Throw Design

To create a single-pole, double-throw (SPDT) switch that can be used as a T/R switch at the antenna, two series-shunt configurations were combined. Figure 2.10, shows the schematic of the SPDT switch. Focusing on the left side of this circuit when A is high and B is zero, the anode of the series diode is at a high voltage and the cathode is DC grounded so it turns on. The shunt device is reverse biased so it presents a large impedance to the signal path. Thus, the RF signal is able to flow from port 1 to 2, as shown in blue. The right side of the circuit is just the opposite when A is high and B is zero. The shunt diode turns on, but the series diode is off so very little RF signal flows from port 1 to 3. In a similar fashion, to direct the RF energy from port 1 to 3 (shown in green), A is set to zero and B is high.

Decoupling capacitors were added to the A and B inputs to provide a good on chip AC ground. In addition, a current limiting resistor R_1 was added to reduce the power

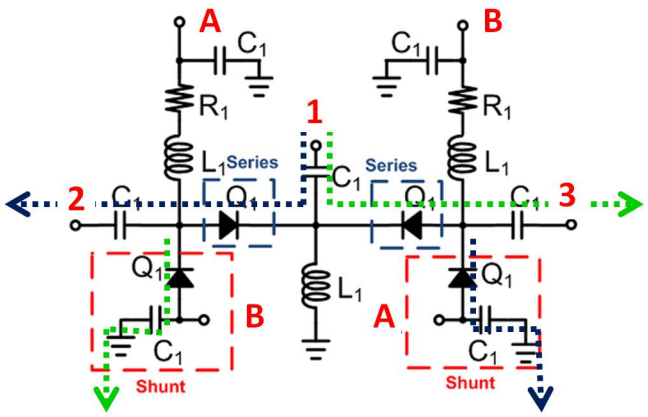

Figure 2.10: Single-pole, double-throw schematic.

consumption. Choosing the value of the resistor R_1 highlights the tradeoff between insertion loss and power consumption. Adding R_1 creates a small voltage drop so that the voltage over the diode is no longer equal to the optimum bias voltage of 0.95 V. While this decreases the insertion loss some, Figure 2.9 shows good insertion loss is still achieved with the anode of the series device at 0.9 V. By decreasing the bias from 0.95 V to 0.9 V, the diode operates at significantly reduced current bias and power consumption. The resistor also helps to provide broadband matching characteristics. Figure 2.11 displays the insertion loss and power consumption of the SPDT for several different resistor values. Based on this tradeoff, R_1 was selected to be 12 ohms.

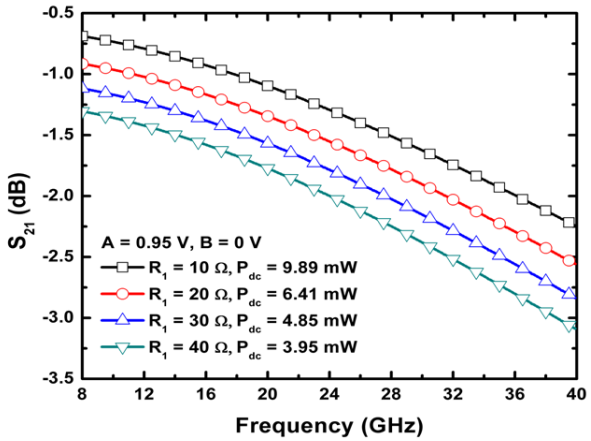

Figure 2.11: Tradeoff between insertion loss and power consumption.

The inductor value was sized for a wideband match. To maximize the performance over an 8-40 GHz bandwidth, the inductor was chosen so the return loss peaked at 24 GHz. Figure 2.12 shows the optimum value of this inductor is 1.2 nH.

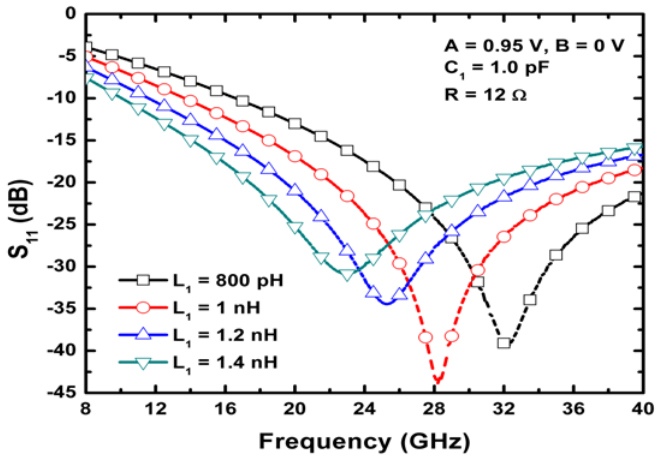

Figure 2.12: Selection of inductor value.

Figure 2.13 is a photomicrograph of the fabricated die. The circuit measures 1.38 x 0.99 mm^2 with pads and 0.48 x 0.41 mm^2 without pads. The layout includes two sets of A and B pads to facilitate easy measurement. In addition, if the circuit were flip-chipped, placing solder bumps on all four sides would improve the planarity. The switch consumes 5.6 mW of power.

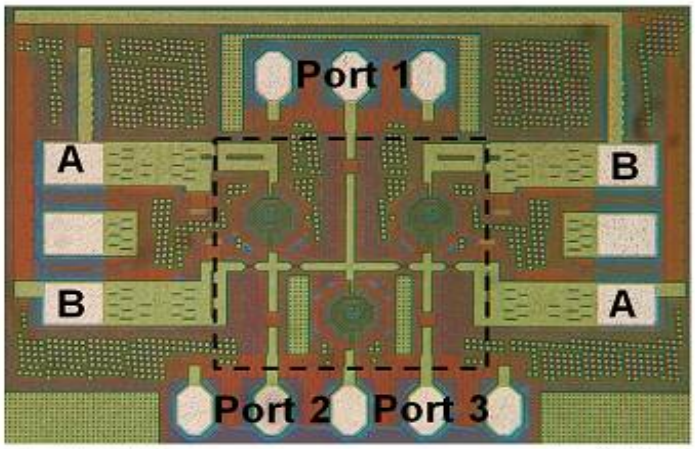

Figure 2.13: Photomicrograph of the fabricated SPDT switch.

The parasitic extracted simulation and measured results are shown to be in good agreement in Figure 2.14. The insertion loss varies from 1.6 to 4.3 dB and the isolation is from 20.3 to 58 dB over 8-40 GHz. The return loss is better than 9 dB over the entire frequency range.

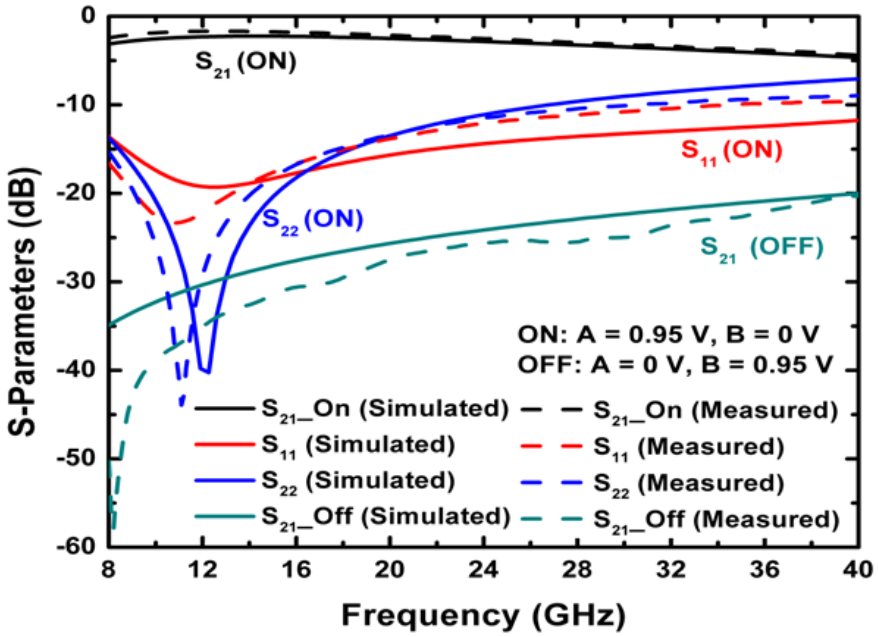

Figure 2.14: Measured and parasitic extracted S-parameters for SPDT switch.

The measured and extracted results show the return loss shifted to lower frequencies in comparison to the ideal case in Figure 2.12. This shift was caused by the parasitic capacitances associated with the transmission lines. The measured power consumption was also noticeably reduced from the value estimated when the limiting resistor was selected. This discrepancy is the result of parasitic trace resistances which create a bigger voltage drop between the bias pad and the diode. This causes the diode to operate at a lower voltage and reduces power consumption. In future work, re-optimizing the matching network after including EM simulations of the transmission lines could improve the return loss.

CHAPTER III

LOW-NOISE AMPLIFIER

The block diagram of the phased-array radar system in Figure 1.7 shows the LNA is a key block in the receiver. The simultaneous requirements for low noise, high gain, power matching, and linearity make the LNA a challenging circuit to design. Most LNAs contain only a couple transistors because each transistor adds more noise to the system. The most common LNA architectures are shown in Figure 3.1. The common emitter topology offers good gain and noise figure, but is inherently limited in terms of bandwidth. The common base topology tends to achieve better linearity and bandwidth, but has a higher noise figure [21, 27]. The third topology is a cascode configuration. The cascode topology is essentially a common emitter amplifier in which the output signal is fed into a common base.

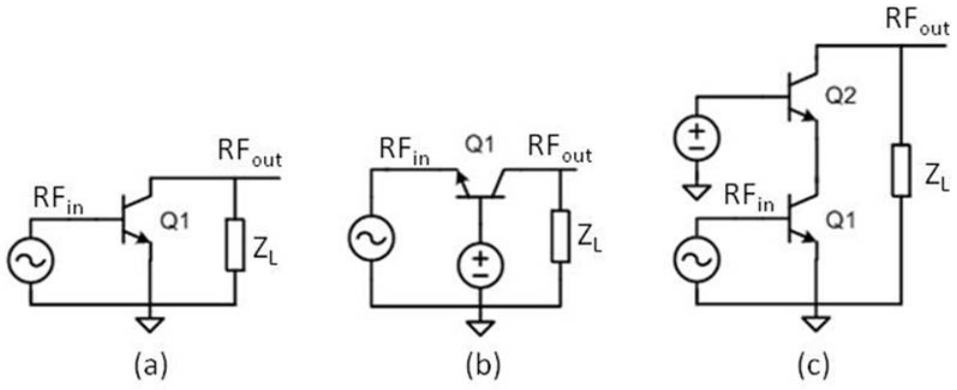

Figure 3.1: LNA topologies: (a) Common emitter (b) Common base (c) Cascode.

The cascode architecture is selected for this work for several reasons. First, the common emitter stage provides a large gain and good noise figure. As a result of the large gain, the effect of the noise added by the second common base transistor is small.

In addition, the low impedance looking into the emitter of the upper transistor limits the impact of the miller capacitance on the common emitter stage [18]. This increases the amplifier performance at high frequencies. The upper transistor also helps to isolate the input from output. This is especially useful in reconfigurable circuits because it reduces the effect a changing the input matching network has on the output impedance. Finally, the cascode offers benefits over a two-stage amplifier because it re-uses the same current path to bias both the common emitter and common-base and thus reduces power consumption.

3.1 Amplifier Stability

The importance of a thorough stability analysis is often underestimated in amplifier design. Rollett's K-factor analysis is by far the most common stability test for RF amplifier design. However, the K-factor analysis has little meaning without proper modeling of parasitics and external components such as pads, probes and contact resistances. In addition, there are circuits where the K-factor analysis is insufficient to guarantee stability. In this section, the basic theory behind the K-factor analysis is reviewed from a conceptual standpoint. The limitations of the K-factor analysis are discussed and an alternative approach is described. This information is then incorporated into the design of a cascode LNA.

3.1.1 Rollett's K-factor Analysis

Rollett's K-factor analysis was originally developed to create a measure of stability independent of the passive terminations connected at the input and output [28]. Rollett's work provided the basis for several different stability criteria developed specifically for S-parameter networks and RF amplifiers [39, 8, 3]. While beneficial when used properly, the different stability metrics can make literature difficult to fully grasp. This introduction into K-factor analysis briefly describes the underlying theory and resolves the differences in stability metrics.

The basic amplifier architecture is shown in Figure 3.2. The active device is matched to the source and load impedances through matching networks. Looking out of the input of the active device, the input matching network causes some of the propagating RF wave to be reflected back towards the active device. The ratio of this reflection to the incident wave is defined by the source reflection coefficient Γ_S. Similarly the output matching network has an associated load reflection coefficient Γ_L. Γ_{in} and Γ_{out} represent the reflection coefficients looking into the active device at the input and output. Reflection coefficients can be mapped to corresponding impedances and vice versa as defined in Equations (3.1) and (3.2).

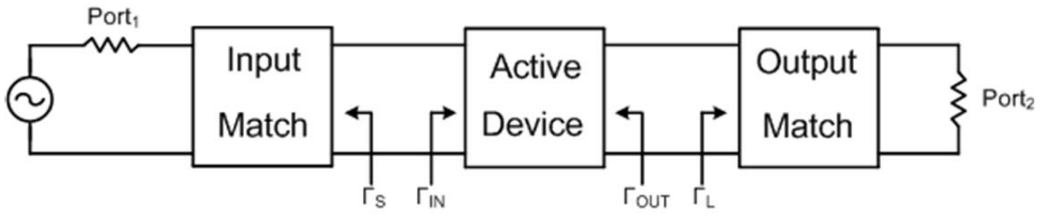

Figure 3.2: General amplifier circuit.

$$Z = Z_0 \frac{1+\Gamma}{1-\Gamma} \tag{3.1}$$

$$\Gamma = \frac{Z - Z_0}{Z + Z_0} \tag{3.2}$$

Any active device can be estimated by its corresponding S-parameters. When the device is terminated with some arbitrary load impedance Z_L (or equivalently Γ_L), it can be represented by the signal flow graph shown in Figure 3.3. Using the signal flow graph and feedback theory, Γ_{in} can easily be derived to Equation (3.3). In a similar fashion, Γ_{out} can be defined for a given source reflection coefficient as seen in Equation (3.4).

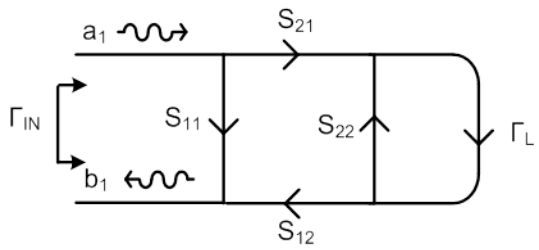

Figure 3.3: Signal flow graph of an amplifier with a load termination.

$$\Gamma_{in} = \frac{a_1}{b_1} = S_{11} + \frac{\Gamma_L S_{21} S_{12}}{1 - \Gamma_L S_{22}} \tag{3.3}$$

$$\Gamma_{Out} = S_{22} + \frac{\Gamma_S S_{21} S_{12}}{1 - \Gamma_S S_{11}} \tag{3.4}$$

In order to be unconditionally stable, Γ_{in} and Γ_{out} must be less than unity for all passive source and load terminations (Γ_S, Γ_L). Passive terminations always have some positive resistance (parasitics always exist) and thus from Equation (3.2) have a $|\Gamma| < 1$. If Γ_{in} or Γ_{out} is greater than unity for any $|\Gamma_S|$, $|\Gamma_L| < 1$, then the amplifier is potentially unstable. According to Equation (3.1), a $|\Gamma| > 1$ corresponds to a negative impedance, which can lead to oscillations.

Equation (3.3) can be rearranged so that Γ_L is a function of Γ_{in}. The stability borderline occurs when $|\Gamma_{in}| = 1$. This can be mapped onto a set of Γ_L points for which $|\Gamma_{in}| = 1$. Setting the absolute value of Equation (3.3) equal to unity and solving for Γ_L, the stability borderline is found to be a circle in the Γ_L-plane, as seen in Figure 3.4. To visualize the Γ_L-plane, a Smith chart is utilized. The Smith chart maps impedances to corresponding reflection coefficients where constant impedances and reactances are partial circles in the Γ_L plane.

This plot is known as the output stability circle and can be used to determine if a given load impedance (Γ_L) creates a reflection coefficient greater than unity at the input. The interior of the stability circle may represent $|\Gamma_{in}| < 1$ or $|\Gamma_{in}| > 1$

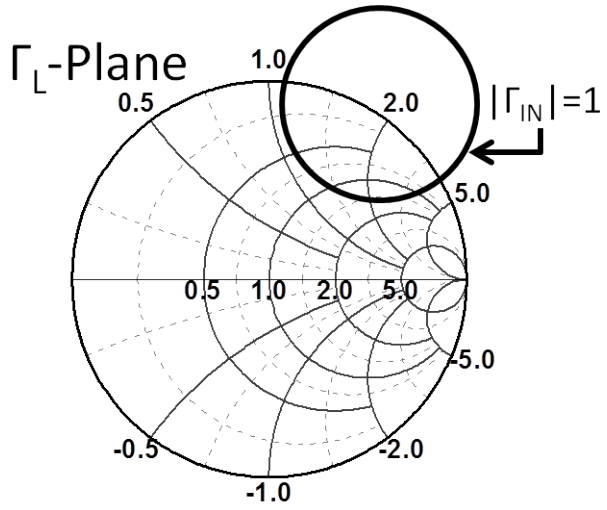

Figure 3.4: Output stability circle in the Γ_L-plane.

depending on the specific network. To determine whether the inside or the outside of the circle represents the stable region ($|\Gamma_{in}| < 1$), a test point is used. Usually, the characteristic impedance Z_0 is used as the test point so $\Gamma_L = 0$ and $\Gamma_{in} = S_{11}$. In this way, it can easily be determined if the inside or the outside of the circle represents stable region by checking $|S_{11}| < 1$. Figure 3.5 shows the four possible stability cases.

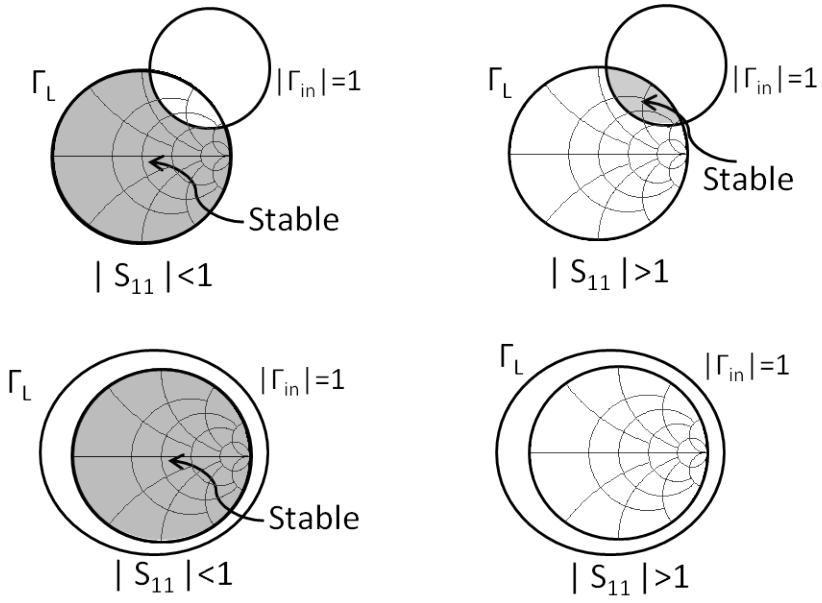

Figure 3.5: Four possible stability cases.

If both the output (Γ_L-plane) and input (Γ_S-plane) stability circles show there are no passive terminations (Γ_L,Γ_S) that can make that Γ_{in} or Γ_{out} greater than one, then the amplifier is unconditionally stable. If this is not true, then the amplifier is potentially unstable. It is important to realize, that just because a Γ_L creates an input reflection coefficient greater than unity, it does not necessarily mean the circuit is unstable. It only indicates that there exists some source impedance such that the conditions for oscillation are met. For other source impedances, the circuit may actually be stable.

To derive the requirements for unconditional stability, the Γ_{in}-plane must be analyzed. Similar to mapping the Γ_{in} borderline onto the Γ_L-plane, all possible passive load impedances can be mapped on to the Γ_{in}-plane [26]. This transformation is shown in Figure 3.6, where the center and radius of the circle are given in Equations (3.5) to (3.7).

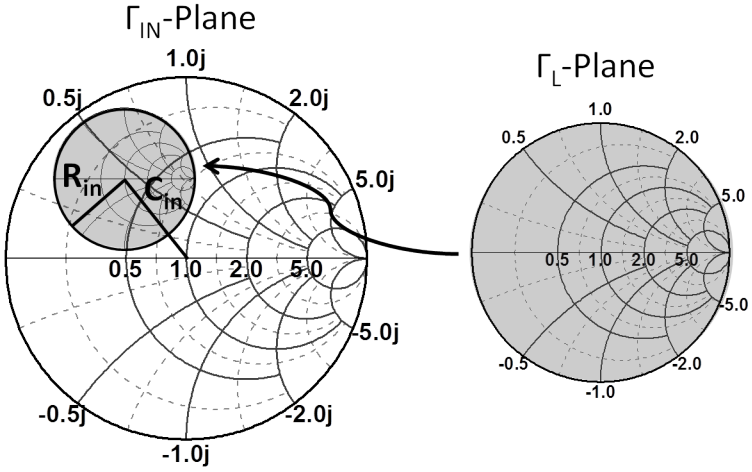

Figure 3.6: Impedance transformation from the Γ_L to the Γ_{in}-plane.

$$C_{in} = \frac{\Delta S_{22}^* - S_{11}}{1 - |S_{22}|^2} \tag{3.5}$$

$$R_{in} = \frac{|S_{12}S_{21}|}{1 - |S_{22}|^2} \tag{3.6}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{3.7}$$

In order to meet stability requirements and have the input reflection coefficient less than unity for all load impedances, Equation (3.8) must be satisfied. To simplify the absolute value relationship, both sides of the equation are squared as shown in Equation (3.9). Using the expressions for C_{in} and R_{in}, Equation (3.9) can be simplified to the condition in Equation (3.10), which is known as the K-factor.

$$|C_{in}| + R_{in} < 1 \tag{3.8}$$

$$|C_{in}|^2 < (1 - R_{in})^2 \tag{3.9}$$

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2\,|S_{21}S_{12}|} > 1 \tag{3.10}$$

There are several benefits to having the K-factor in this form. First, the K-factor determines if the load impedance circle intersects the edge of the Γ_{in} Smith chart, indicating possible instability. The K-factor is also only a function of the raw S-parameters, and not a function of the load or source impedances. This intuitively makes sense since the K-factor tests for unconditional stability which covers all possible load and source impedances. Furthermore, the K-factor is symmetric in that if the input port and output port are exchanged ($S_{11} \Leftrightarrow S_{22}$,$S_{12} \Leftrightarrow S_{21}$), the result is the same. This means that if the K-factor is derived from the source impedance

circle, the same result is discovered. Hence, the K-factor indicates unconditionally stability for both input and output.

It is important to note that by squaring both sides in Equation (3.9), an extraneous solution has been added in which $R_{in} > 1$. For this reason, a second condition must be imposed on the stability criteria to reject the false solution. While the K-factor formula represents the mathematical intersection of two circles, the second criteria is just used to remove the extraneous solution. To accomplish this, several different conditions can be used which are not necessarily mathematically equivalent, but all remove the incorrect solution. Equations (3.11) to (3.15) are popular forms of the second criteria. If the K-factor condition is satisfied and one of the secondary criteria is true, then the remaining secondary criteria are also true [22].

$$|\Delta| < 1 \qquad [39] \tag{3.11}$$

$$B_{1f} = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 > 0 \qquad [3] \tag{3.12}$$

$$B_{2f} = 1 + |S_{22}|^2 - |S_{11}|^2 - |\Delta|^2 > 0 \qquad [3] \tag{3.13}$$

$$|S_{12}S_{21}| < 1 - |S_{11}|^2 \qquad [19] \tag{3.14}$$

$$|S_{12}S_{21}| < 1 - |S_{22}|^2 \qquad [19] \tag{3.15}$$

There has also been some effort to combine the two stability criteria into one metric. The μ-test indicates stability with a single equation. However, the μ-test equation is not symmetric and as a result there are two separate values for μ_{in} and

μ_{out}, given in Equations 3.16 and 3.17 [8]. While these values are different, they are either both stable or both unstable at the same time. One benefit of the μ-test is that a larger μ value indicates a great degree of stability. This is not true for the K-factor analysis. The μ value actually represents the distance from the center of the Smith chart to the closest unstable impedance and provides some measure of how far the amplifier is from the stability boundary [13].

$$\mu_{in} = \frac{1 - |S_{22}|^2}{|S_{11} - \Delta S_{22}^*| + |S_{12}S_{21}|} > 1 \tag{3.16}$$

$$\mu_{out} = \frac{1 - |S_{11}|^2}{|S_{22} - \Delta S_{11}^*| + |S_{12}S_{21}|} > 1 \tag{3.17}$$

3.1.2 Limitations of the K-factor analysis

While the K-factor analysis is a good starting point, there are several weaknesses to using this approach. First, the K-factor only analyzes the stability of the input and output for stability and treats the amplifier as a black box. This is usually sufficient for single stage amplifiers, but for amplifiers with multiple active devices, internal nodes can be unstable without failing the K-factor analysis. In addition, the K-factor only indicates when a negative impedance is presented to the input or output. It does not necessarily state if the circuit oscillates. For instance, if 50 Ω ports are placed at the input and output, $\Gamma_S = \Gamma_L = 0$ and according to Equations (3.3) and (3.4), $\Gamma_{in} = S_{11}$ and $\Gamma_{out} = S_{22}$. In this case, the amplifier fails the K-factor stability criteria whenever $S_{11} > 1$ or $S_{22} > 1$. However, devices occasionally have $S_{11} > 1$ or $S_{22} > 1$ at high gain bias points and are found not to be oscillating. The K-factor cannot actually determine if a specific circuit will oscillate; it can only specify that it is impossible for certain circuits to oscillate. Thus, it is quite possible for an amplifier to fail the K-factor test, but not oscillate for a given set of terminations.

In multiple transistor amplifiers, the K-factor analysis is still often used. It is important to understand what the K-factor tests for in such a circuit. One common approach is to simply run K-factor analysis as if the entire amplifier is a single 2-port black box, as it is done for a single transistor. This tests if a negative impedance can be generated at the input or output for all passive source and load terminations. It does not provide any information on the stability of internal nodes. Thus, this approach is *required* for unconditional stability but is *not sufficient*.

Another approach is to split multi-transistor amplifiers into stages and run the K-factor analysis on each stage separately. In this case, each stage is tested to see if it creates a negative impedance for any passive source or load termination. Figure 3.7 illustrates how the impedances at the input and transformed to impedances at the internal node.

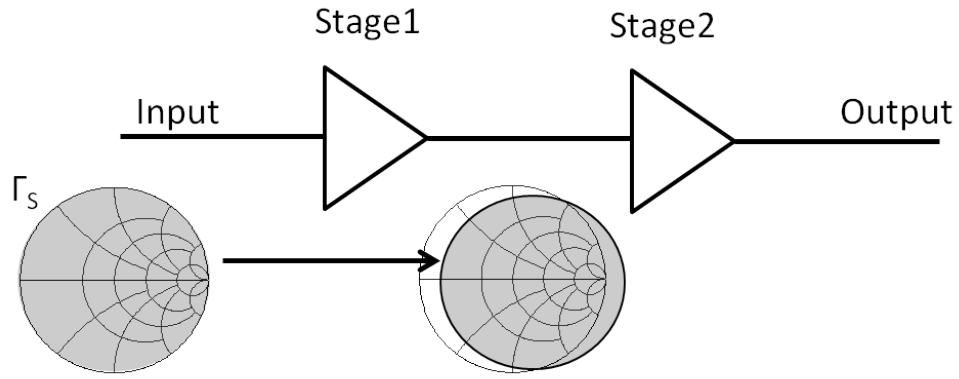

Figure 3.7: Multi-stage amplifier impedance transformation.

The impedance presented by the first stage to the second stage could in fact be a negative impedance. This possibility is not covered when K-factor analysis is run separately for each stage. Furthermore, when the second stage is connected to the first stage, the loading effect of the first stage may prevent the second stage from seeing all possible passive terminations. For instance, in Figure 3.7 the short circuit falls outside the region of impedances presented to the second stage. However, this impedance is still tested in the K-factor analysis of the second stage. This means that

for an individual stage, the K-factor criteria are in fact *not required* and *not sufficient* to determine the unconditional stability of one transistor within a multi-stage design.

The K-factor of an individual stage provides little information, but if every stage is separately unconditionally stable, then the overall amplifier is also unconditionally stable. If this occurs, then the impedance transformation of all passive terminations from the source of the first stage to the source of the second stage stays within the Smith chart as shown in Figure 3.8. In this case, the possible impedances presented at each stage are covered by the K-factor analysis. This is a good indication of stability, but the stage-to-stage feedback is not taken into account. In addition, in topologies like the cascode pair, it may be difficult to separate individual stages properly.

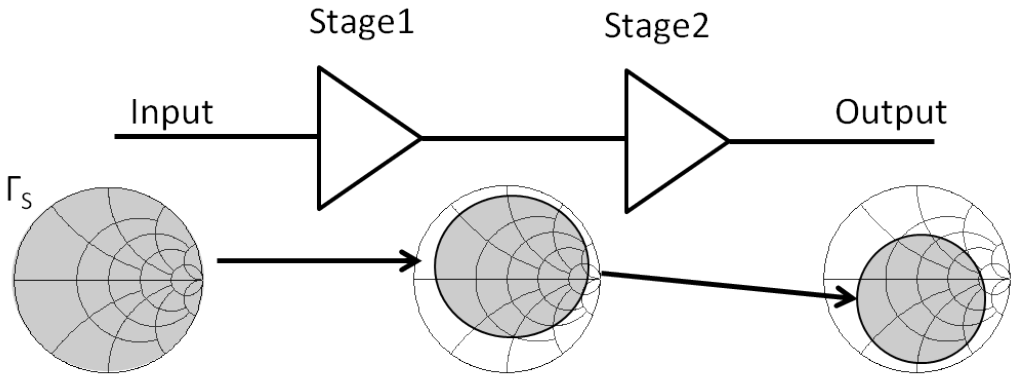

Figure 3.8: Multi-stage amplifier indicating stable operation.

3.1.3 S-Probe Analysis

The S-Probe or Gamma Probe analysis is an alternative to the K-factor that was developed by Texas Instruments in the early 90s [37]. The idea of the S-probe technique is to insert a test circuit which extracts the reflection coefficient looking into and out of any node without changing the circuit performance. In this way, all feedback paths are accounted for in the analysis. The S-Probe test circuit is now available as a component in both Advanced Design Systems and Microwave Office, and can be easily implemented in simulation. The details of this test circuit can

be found in [4]. Once the reflection coefficients are extracted, they can be checked against Nyquist's stability criteria.

To understand the power of the S-probe analysis, consider the network shown in Figure 3.9. This network represents the reflection coefficient looking into and out of any arbitrary node in the circuit. If this network is considered to be a loop over an infinitely small line length, then there are no losses between the two reflection coefficients. In addition, the components that are represented by Γ_1 generate some small thermal noise (v_t). The thermal noise from the Γ_1 network travels towards Γ_2 and is reflected back with the magnitude of $|\Gamma_2 v_t|$. This noise continues to reflect back and forth between the two ports. If the gain in one cycle between the two ports is greater than unity and there is no net phase change, then the noise can quickly grow towards infinity and cause oscillations. In reality, as the signal grows, the active devices are pushed into large signal operation and the reflection coefficients change. This change may or may not result in steady-state oscillations, but regardless it is a situation that should be avoided. The conditions for this type of instability can be expressed using Equations (3.18) and (3.19).

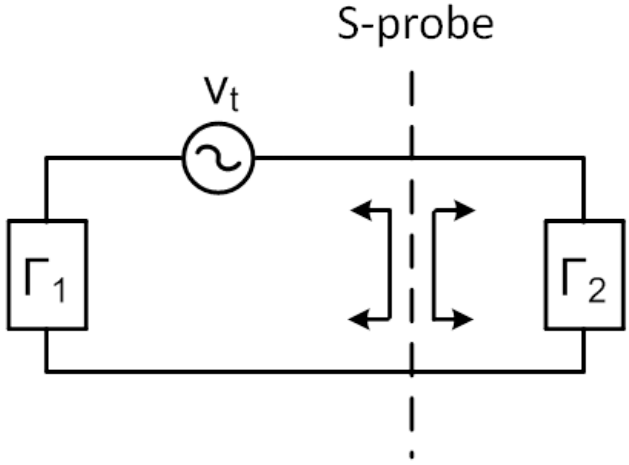

Figure 3.9: S-probe circuit model for any arbitrary node.

$$|\Gamma_1 * \Gamma_2| > 1 \tag{3.18}$$

$$imag\,(\Gamma_1 * \Gamma_2) = 0 \tag{3.19}$$

An equivalent test to the conditions in Equations (3.18) and (3.19) is to use a polar plot of $\Gamma_1 * \Gamma_2$ and check if the point (1,0) is encircled in a clockwise fashion (Nyquist plot). Figure 3.10 shows an example Nyquist plot where the node is stable since the (1,0) point is not encircled. Some simulators will further simplify these criteria and use just Equation (3.18), which causes some false-positive cases, but can easily be included as a Boolean requirement in optimization schemes.

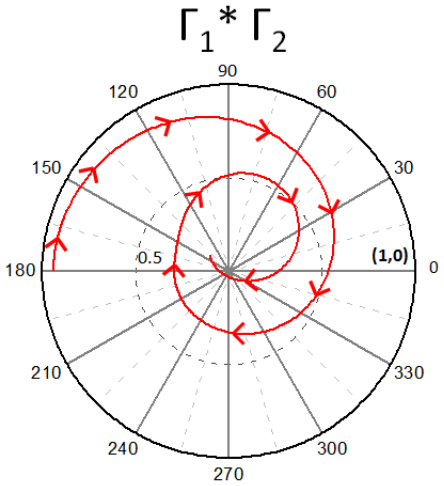

Figure 3.10: Example Nyquist plot.

Using the S-Probe technique, the potential for oscillations at any given node can be determined for specific source and load terminations. This is very helpful for circuits with multiple active devices in which the K-factor analysis provides limited information. In fact, the K-factor is really just a special case of the S-probe analysis. Figure (3.11) illustrates how the S-Probe analysis can be used to generate the K-factor results. If an S-probe is placed at the input of the amplifier and Γ_1 represents

all the passive source impedances ($\Gamma_1 = \Gamma_S < 1$), then the S-probe stability condition reduces to $\Gamma_2 < 1$, where in this case $\Gamma_2 = \Gamma_{in}$. A similar analysis at the output leads to $\Gamma_{out} < 1$. The requirements of $\Gamma_{in} < 1$ and $\Gamma_{out} < 1$ are the fundamental conditions for which the K-factor is derived. Thus the K-factor is a special case of the S-probe analysis in which all passive source and load terminations are considered.

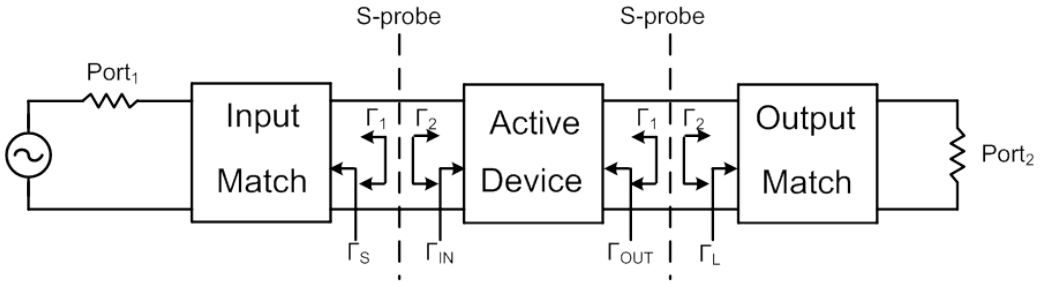

Figure 3.11: General amplifier with S-probes at the input and output.

To ensure that a circuit will not oscillate, the S-Probe simulation should be checked at each terminal of the active devices. Passive components cannot create reflection coefficients greater than one because they always have some positive parasitic resistance. The S-probe simulation should be run for a large number of source and load impedances to determine unconditional stability. Testing terminations on the edge of the Smith chart checks the worst case scenarios since Γ_S and Γ_L are very large. It is important to investigate frequencies from DC all the way up to f_{max}. Low frequency oscillations may mix with other frequency signals to produce problems in-band. A thorough analysis will also run the S-Probe analysis over a wide range of operating temperatures and current gains, β.

The S-Probe theory can shed light on good design practices. Often designers include small resistors on DC bias lines. Large capacitors are normally used to decouple DC bias nodes, but at RF frequencies these nodes look like short circuits. From a stability stand point this can be very damaging since the magnitude of the reflection coefficient of a short circuit is 1. Based on the S-Probe theory, if the reflection

coefficient looking out of that node is greater than unity and of opposite phase, oscillations can start. However, by adding a small resistance to the bias node before the decoupling capacitor, the reflection coefficient is reduced. Using the same logic, it follows that the DC bias point of an RF circuit should not be measured without probing down on the RF pads. If the RF probes are disconnected from the circuit, then the input and output are open circuits. This is a worst case stability scenario in which all the noise energy is reflected back towards the circuit and could cause damaging oscillations. The stability of the cascode topology is analyzed in detail in the next section.

3.2 Narrowband Design

A simple narrowband LNA was developed to provide a basis of comparison for reconfigurable designs. This design was also used to develop the design flow and provide insight into the tradeoffs associated with a cascode LNA. The approach used in this work achieves a simultaneous noise and power match at the input, while balancing noise figure and gain. The basic schematic of this design is seen in Figure 3.12.

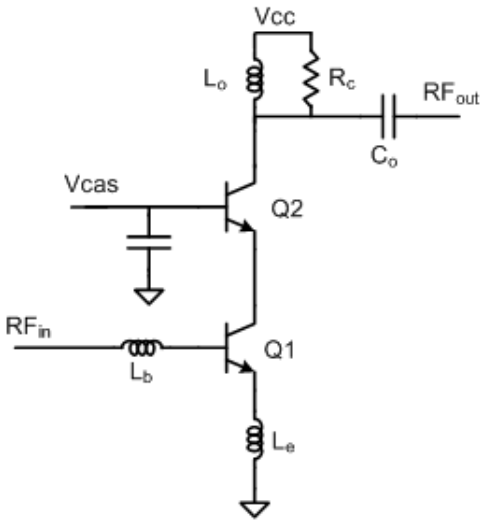

Figure 3.12: Schematic of the narrowband LNA.

The procedure to achieve a simultaneous noise and power match at the input is described thoroughly in [34]. The collector current density is selected based on the tradeoff between noise figure and gain. The transistor is sized so the real part of the optimum noise match is 50 Ω. An emitter degeneration inductor is added to match the real part of the input impedance to 50 Ω. Finally, a base inductor is used to cancel the reactance and match both the optimum noise and input impedances to 50 Ω. The simulation results in Figure 3.13 show this procedure achieves both a good power and noise match at 10 GHz.

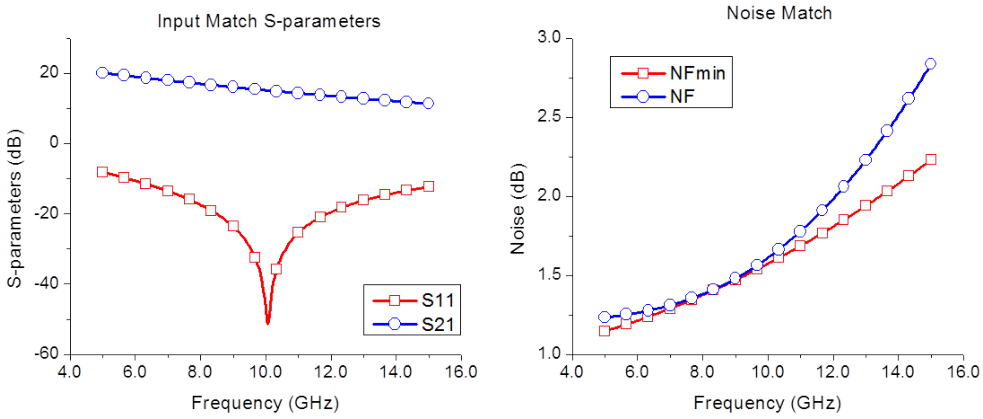

Figure 3.13: Simulation of the LNA input match.

At the output, the cascode topology has a very high output resistance and it is hard to match to 50 Ω. To achieve a match, a resistor is added from the collector to the voltage supply. From an RF stand point, this resistor is a parallel load impedance between the output node and RF ground. The resistor reduces the output resistance, making the matching network more practical. The output match is completed with an LC network (L_o and C_o), as shown in Figure 3.12. The inductor L_o also provides a DC current path for biasing.

The simulated S-parameters including the output match are shown in Figure 3.14. While the input return loss is still quite good, it is clear that adding the output matching network degraded the impedance match at the input. This is because the

input and output are not completely isolated from one another. The circuit could be re-optimized to improve the input match, but this usually requires larger inductors and degrades the noise figure.

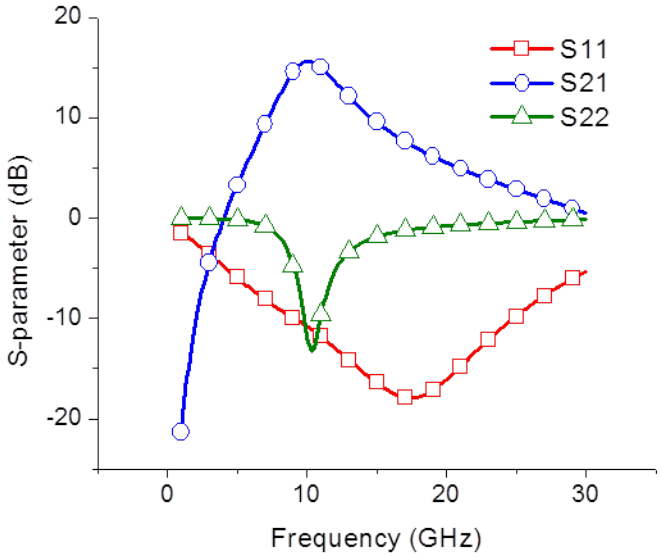

Figure 3.14: Simulation of the complete LNA S-parameters.

3.2.1 Cascode Topology Stability

A combination of the K-factor and S-probe analyses provide the tools necessary to evaluate the stability of a multi-transistor amplifier. The cascode topology used for the LNA described in this work is notorious for causing stability issues. In particular, the stability at the base node of the upper (cascode) transistor is of concern [1]. The impedance looking into the base of the cascode can be derived using the diagram in Figure 3.15. The lower transistor has been modeled as a capacitive load, which results in the impedance given in Equation (3.20). Separating the impedance into real and imaginary parts, Equation (3.21) shows the real part of the impedance looking into the base can be negative. If the real part of this impedance is negative, the reflection coefficient will be greater than one and the potential for oscillations exists at this node.

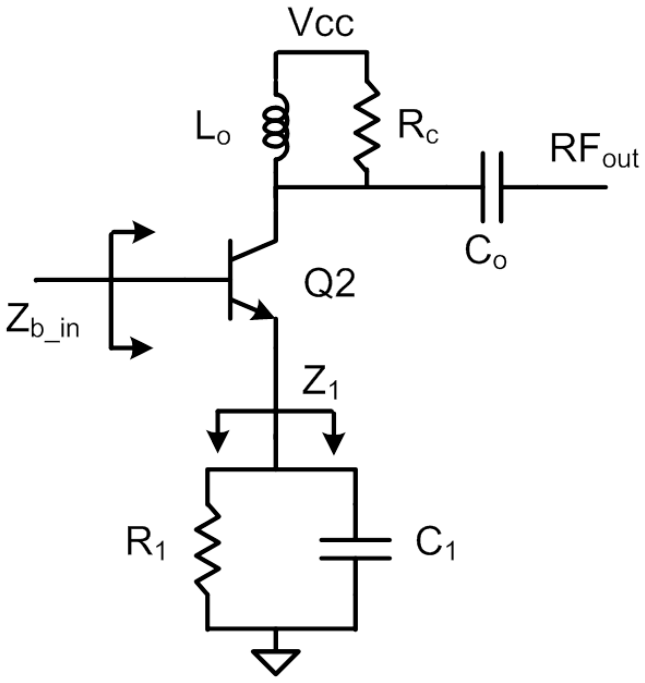

Figure 3.15: Circuit model used to calculate impedance at upper base.

$$Z_{b\_in} = \frac{1}{sC_{be}} + Z_1\left(1 + g_m\frac{1}{sC_{be}}\right) = R_{b\_in} + j * X_{b\_in} \tag{3.20}$$

$$R_{b\_in} = \frac{R_1}{(\omega R_1 C_1)^2 + 1} - \frac{\omega^2 g_m R_1^2 C_1 C_{be}}{(\omega^2 R_1 C_1 C_{be})^2 + (\omega C_{be})^2} \tag{3.21}$$

According to the S-Probe theory, the negative resistance may or may not cause oscillation conditions depending on the impedance looking out of the cascode base. Figure 3.16 shows the application of the S-Probe to the base of the cascode device. In order to obtain valid simulation results, all parasitics, pads, and probes must be included in simulation. To create oscillation conditions, the loop gain must be greater than one and in phase. Unfortunately, looking out of the cascode base, the node is RF grounded and the reflection coefficient is close to 1. Thus, it is quite possible for oscillations to occur on this node when there is a negative resistance looking into the cascode base.

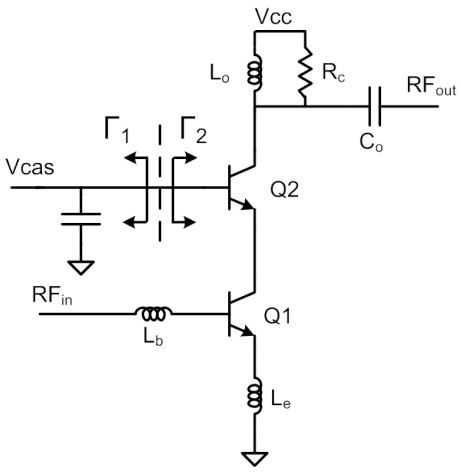

Figure 3.16: S-probe setup for the cascode topology.

Using the S-probe technique, the reflection coefficients at the upper base can be extracted. Figure 3.17 shows the reflection coefficient looking into the cascode base can be much larger than unity.

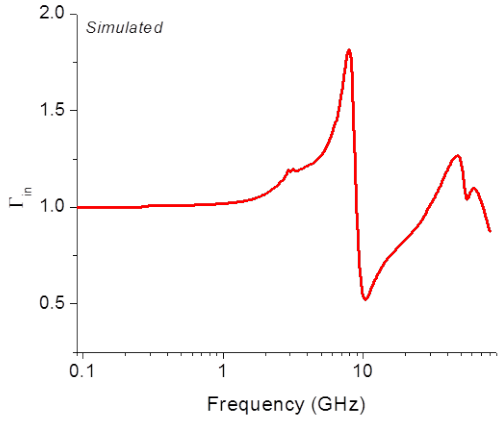

Figure 3.17: Reflection coefficient looking into the cascode base.

Figure 3.18 shows the polar plot of the reflection coefficient product over frequency for a $\Gamma_S = 0.95\angle 300^0$ and $\Gamma_L = 0.95\angle 210^0$. These reflection coefficients were determined to be a worst case scenario for stability and the (1,0) point is encircled in a clockwise fashion indicating that oscillations can exist on this node.

One way to improve the stability at this node is to include a small resistor between

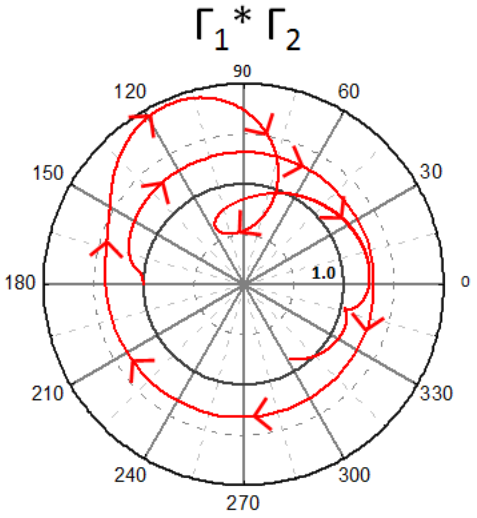

Figure 3.18: Nyquist plot of the upper base node.

the cascode base and RF ground. This reduces the reflection coefficient looking out of the cascode base and decreases the overall loop gain. Figure 3.19 shows the Nyquist plot with a 10 Ω resistor added to the bias line. The product of the reflection coefficients no longer encircles the (1,0) point and indicates the node is stable. The analysis presented here for the cascode base is carried out at each terminal of the active devices. However, normally it is found that the cascode base is the most susceptible to oscillation conditions.

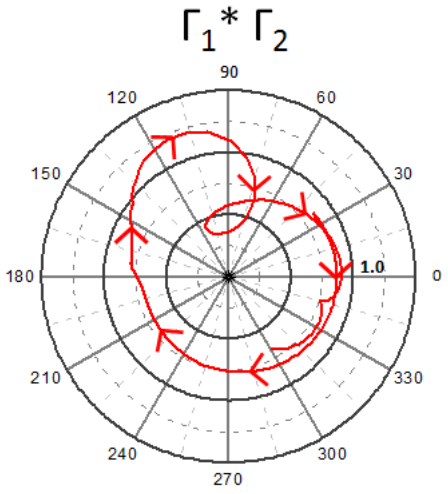

Figure 3.19: Nyquist plot of the upper base node with added resistor.

3.2.2 Measured Results

The photomicrograph of the narrowband cascode LNA is shown in Figure 3.20. The emitter degeneration inductor is split into two inductances from the emitter node to ground. This creates a more symmetrical layout and a more balance current distribution through the transistors. Microstrip transmission lines with a characteristic impedance of 50 Ω are used to connect components together. The final layout measures 1100 μm by 800 μm.

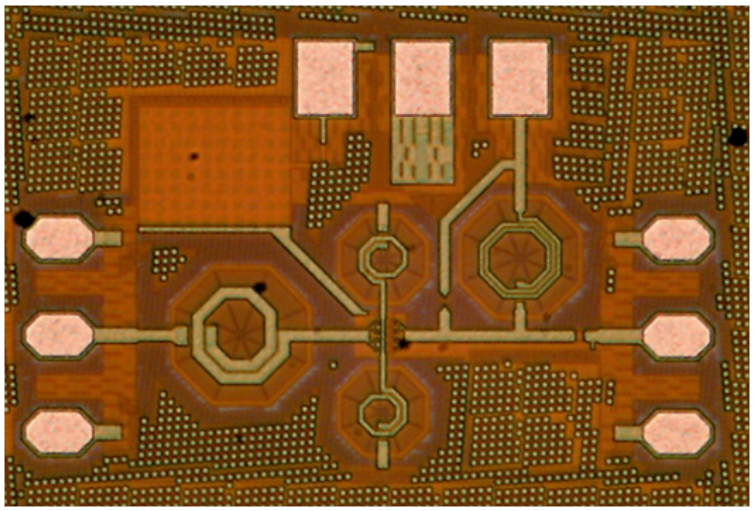

Figure 3.20: Photomicrograph of narrowband LNA.

In measurement, a large shift in the center frequency was observed. It was determined that the voltage supply node did not have sufficient capacitance to provide a good RF ground. As a result, the impedance of the DC probes influenced the circuit response. To reduce this effect, DC probes with 100 pF decoupling capacitors positioned close to the probe tips were used in measurement. The impedance looking into the DC probe was measured with a one port S-parameter measurement. The S_{11} of the DC probe is shown in Figure 3.21. The probe is close to an RF short as expected, but there is still a small impedance and some resonances associated with the probes. In future designs, as much decoupling capacitance as possible will be added to the DC bias nodes to prevent the probe impedance from affecting measurement.

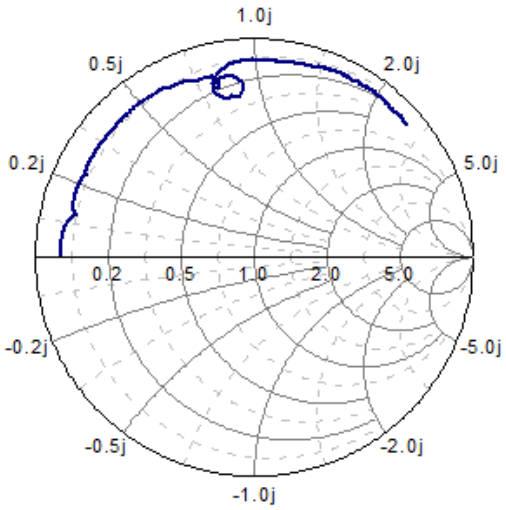

Figure 3.21: Measured probe impedance from 1-40 GHz.

Two main effects caused the center frequency to decrease from initial simulations. First, the parasitic capacitances of the interconnecting transmission lines caused the center frequency to shift from 10 GHz to 9.2 GHz. In addition, when the model for the DC probe was incorporated into simulation, it was found the center frequency decreased from 9.2 GHz to 8.2 GHz. The measured and simulated S-parameters are shown in Figure 3.22. After taking these effects into account, the measured and simulated results are in good agreement. In the future, the decrease in center frequency can be avoided by incorporating EM simulated transmission lines earlier in the design process and having a good on-die RF ground.

The remaining discrepancy between measurement and simulation is attributed to poor modeling and the difficulty of EM simulating inductors with an active ground shield. The inductors in this LNA employed an active ground shield to increase the quality factor. The active ground shield reduces losses through the substrate, but makes it very difficult to accurately EM simulate the inductor. As a result, the inductors may have caused the additional shift in frequency. Further revisions of this design will use inductors with a metal ground shield or no shield to facilitate better EM simulation results.

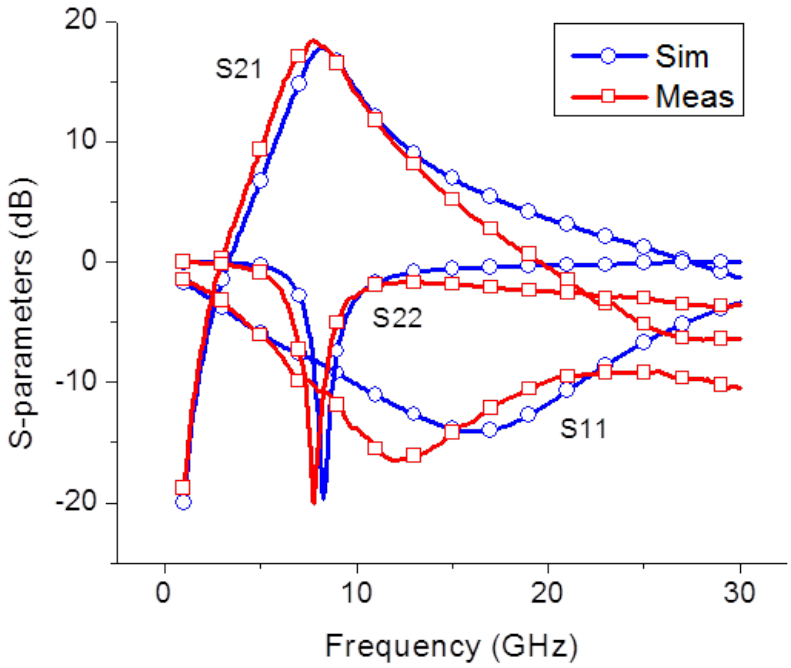

Figure 3.22: LNA measured vs. simulated S-parameters.

3.3 Switchable Transistor Cores

A common design approach for a reconfigurable LNA is to have switchable matching networks or varactors which allow the circuit to change to different frequencies or noise matches [7, 33]. These designs are normally large in size because the switchable networks add a significant number of passive components. In addition, this type of design is limited in its ability to reconfigure to handle higher input powers. An alternative approach is to switch in additional transistors. Figure 3.23 shows the basic concept of having a switchable transistor core. The optimized switches designed in the previous chapter can be used to control the state of the second transistor. The analysis in this work only considers switching in one additional transistor, but the concepts may be extended to designs with many switchable devices.

For a single transistor LNA design, a simultaneous noise and power match can be achieved with inductors at the base and emitter. The bias point, transistor size,

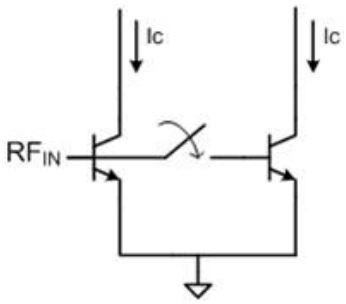

Figure 3.23: Basic switchable transistor core architecture.

and emitter inductor are chosen such that $\frac{g_m}{C_{be}} L_e = 50\,\Omega$. The base inductance is then chosen to resonate out the capacitive load at the operating frequency. Figure 3.24 shows the small signal diagram looking into the LNA, with the input impedance given in Equation (3.22).

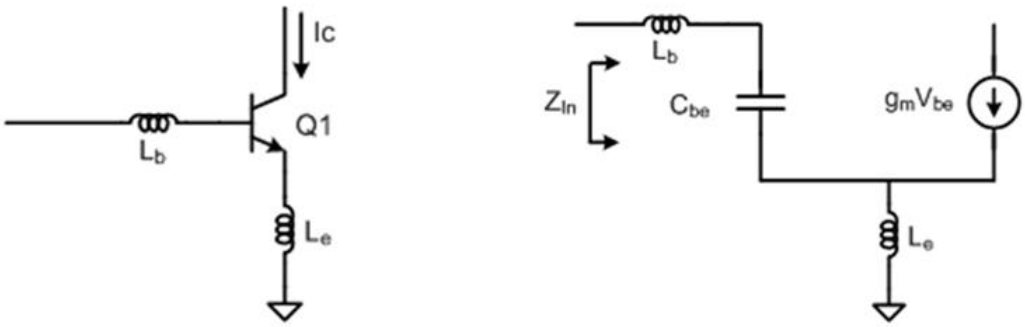

Figure 3.24: Small signal diagram of a single transistor LNA.

$$Z_{in} = \frac{g_m}{C_{be}} L_e + j\left[\omega\left(L_e + L_b\right) - \frac{1}{\omega C_{be}}\right] \tag{3.22}$$

This same approach can be used for a multiple transistor design as seen in Figure 3.25. To simplify the results, the impedance of the switch in between the two transistors is assumed to be relatively small so that $V_{be1} = V_{be2}$. If both transistors are biased at the same current density, then the $\frac{g_m}{C_{be}}$ ratio remains the same when the second transistor is turned on and off. Looking at Equation (3.23), if the $\frac{g_m}{C_{be}}$

ratio remains constant ($\frac{g_{m1}}{C_{be1}} = \frac{g_{m2}}{C_{be2}} = \frac{g_{m1}+g_{m2}}{C_{be1}+C_{be2}}$), then the real part of the input impedance does not change when additional transistors are switched in to operation. With the switch turned on, the imaginary part of the input impedance becomes more inductive as a result of the extra base-emitter capacitance. Equation (3.24), shows the imaginary part of the input impedance resonates out at a lower frequency when the second transistor is turned on. In this way, adding transistor cores can provide frequency tuning [38].

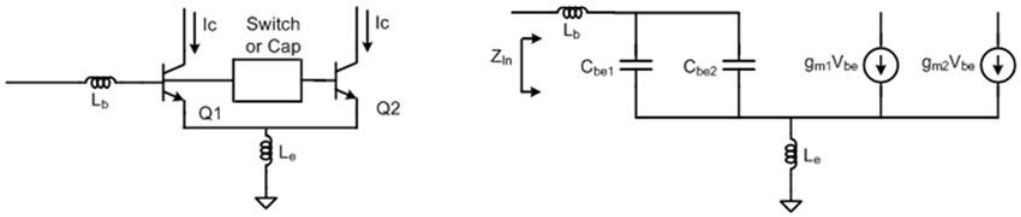

Figure 3.25: Small signal diagram of a switchable transistor LNA.

$$Z_{in} = \frac{g_{m1} + g_{m2}}{C_{be1} + C_{be2}} L_e + j \left[\omega \left(L_e + L_b \right) - \frac{1}{\omega \left(C_{be1} + C_{be2} \right)} \right] \tag{3.23}$$

$$\omega_0 = \sqrt{\frac{1}{\left(C_{be1} + C_{be2} \right) \left(L_e + L_b \right)}} \tag{3.24}$$

This is an encouraging theoretical result, but the assumption that the switch impedance is small enough to ignore is not always accurate and is heavily dependent on how the switch is implemented. Fundamentally, there are three ways to operate this switch. One option is for the switch to turn on and off both the AC and DC current. Alternatively, the DC current could always be present and the switch could just turn on or off the AC current flow. The advantage to this topology is that the switch could include blocking capacitors at the input and output. This would allow the source-bulk and drain-bulk junctions to be reverse biased to decrease the lossy

parasitic capacitances. Finally, a third option is the AC current flow could always be present, but the DC biasing could turn on or off the additional transistors.

In order to implement either the only AC or only DC switch, separate paths for the DC and AC current must be created to decouple their operation. In simulation, it was determined that the only DC switch significantly outperformed the only AC switch in terms of noise figure when implemented in an amplifier. Three topologies shown in Figure 3.26 were selected to be further explored. The first two use switches that conduct both AC and DC current. The last topology uses a capacitor to separate the DC current between the two transistors while allowing the AC current to pass. The additional transistor can be turned on through the second resistive current mirror.

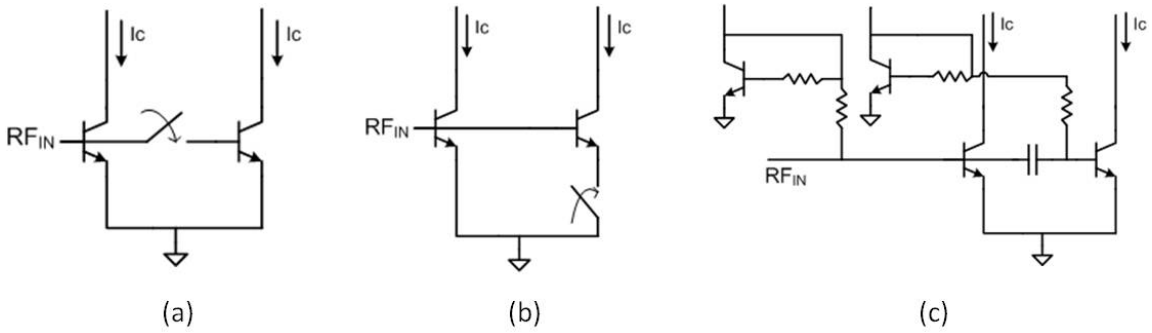

Figure 3.26: Switchable core topologies: (a) Base switch (b) Emitter switch (c)Resistive base bias.

3.3.1 Base Switch Topology

The switch 3.26(a) controls both the AC and DC connectivity between the two transistors. The transistor current density is set by the bias voltage. In this case, the voltage drop over the switch is very low since the base current is small, and both transistors operate at nearly the same current density. As a result the short circuited current gain (H_{21}), which is mainly a function of the current density, remains relatively constant when the switch is turned on and off. However, the loss over the switch increases the noise figure of the transistor core. Figure 3.27 shows the H_{21} and

NF_{min} for the transistor core in the on and off states and compares the results to a single transistor baseline which has no switchable networks.

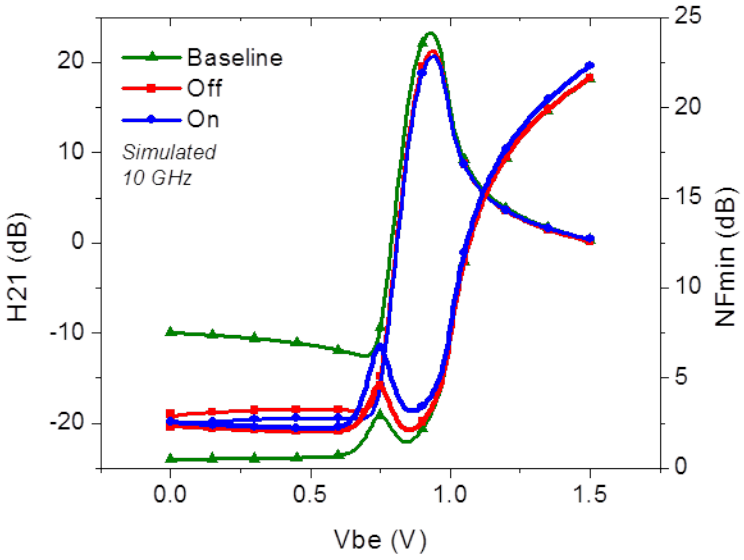

Figure 3.27: Base switch H_{21} and NF_{min} for different V_{be} at 10 GHz.

The additional transistor core adds a parallel impedance, which decreases the input and output impedances. G_{min} is the optimum noise figure impedance and also decreases due to the increase in transistor area. Figure 3.28 shows these effects in simulation at 10 GHz and compares the results to a comparable single transistor core without switchable networks.

Figure 3.29 shows the power handling capabilities of the base switch architecture. The simulation shows the 1dB gain compression point (P_{1dB}) improves by nearly 3 dB from the off to on state. Thus, in this topology switching in another transistor of equal size nearly doubles the power handling capabilities of the amplifier. This could be used to prevent amplifiers from saturating or pushing into the non-linear region of operation.

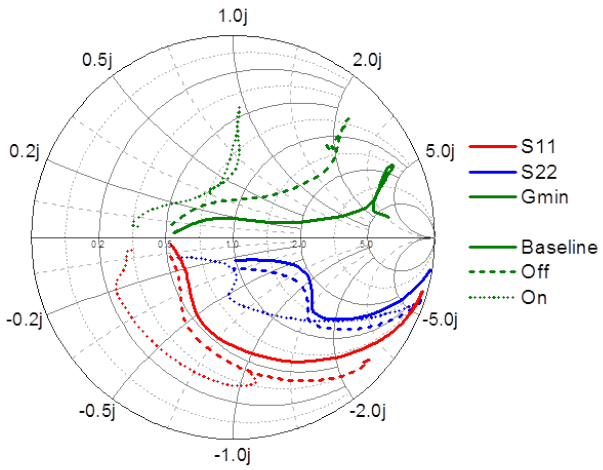

Figure 3.28: Base switch Smith chart at 10 GHz over V_{be}.

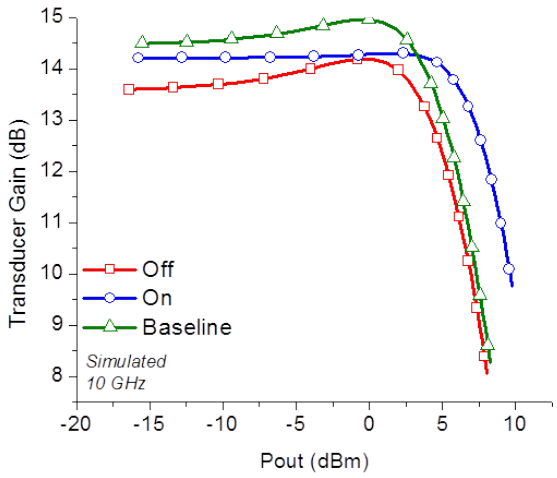

Figure 3.29: Base switch power handling at 10 GHz.

3.3.2 Emitter Switch Topology

A similar analysis was conducted for the emitter switch topology. In Figure 3.30, the plot of H_{21} and NF_{min} shows the noise barely degrades from the baseline case. In the base switch topology, the loss of the switch is multiplied by the gain of the transistor and contributes heavily to the noise at the output of the circuit. However, for the emitter switch, the gain from the emitter to the collector is small so the switch losses have little impact on the overall noise figure.

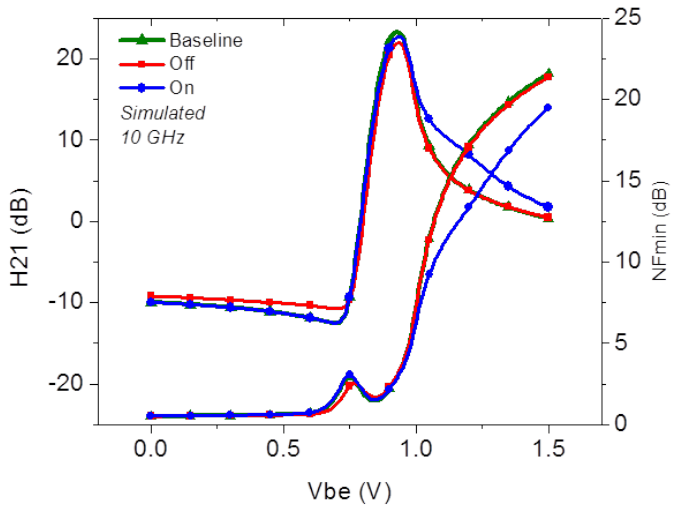

Figure 3.30: Emitter switch H_{21} and NF_{min} for different V_{be} at 10 GHz.

The deviation in the H_{21} and NF_{min} curves in the on state at high voltage bias is the result of current imbalance. When a large current flows through the second transistor, the voltage drop over the switch at the emitter becomes significant. This reduces the V_{be} of the second device and decreases the current flowing through the second transistor. Since the two transistors are operating at different bias points, the H_{21} and NF_{min} plots are distorted from the single transistor case. This is not a problem for the base switch topology because the current flowing through the base is small enough that the voltage drop is negligible.

The Smith chart of the emitter switch topology, in Figure 3.31, shows the real part of S_{11}, S_{22}, and G_{min} shift slightly to lower resistances, but the imaginary parts of the impedances are relatively unaffected. In a reconfigurable design, the input match could be optimized for an impedance in between the on and off states. Then turning the switch on and off could change the power handling performance while maintaining a good noise figure and input match. The P_{1dB} of the transistor core increases by about 1 dB when the second transistor is turned on, and the gain increases by 2 dB, as shown in Figure 3.32.

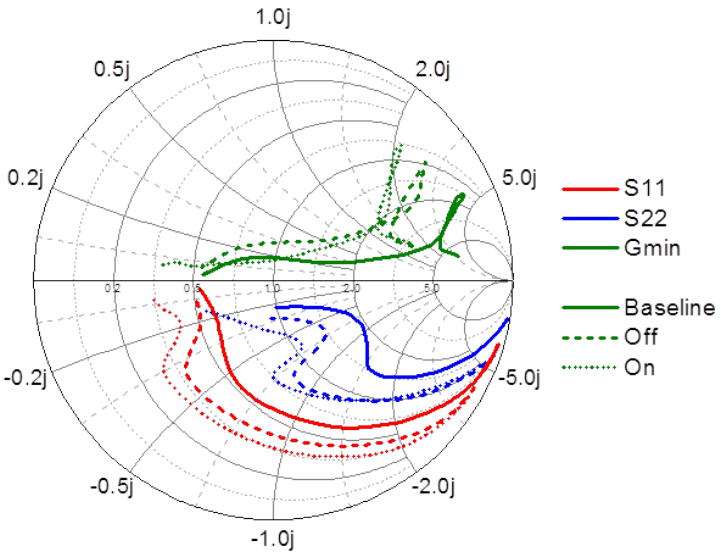

Figure 3.31: Emitter switch Smith chart at 10 GHz over V_{be}.

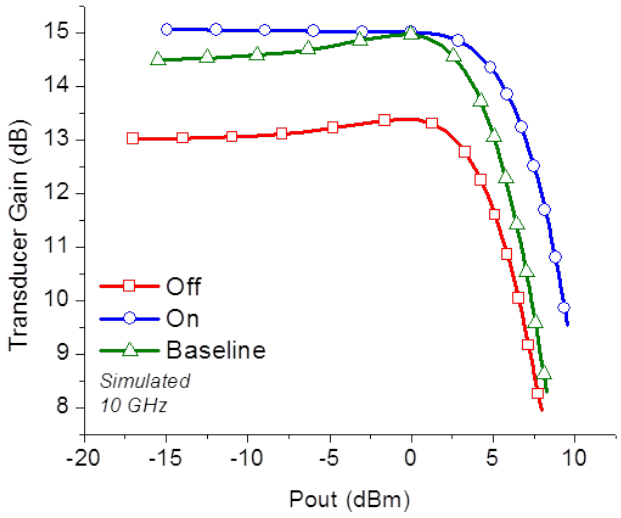

Figure 3.32: Emitter switch power handling at 10 GHz.

3.3.3 Resistive Base Bias Topology

The third resistive base biasing topology is different in that AC current is always flowing into the additional core. By forcing the voltage at the base of the additional transistor to zero, that path can be effectively blocked. Figure 3.33 shows the H_{21}

and NF_{min} for the resistive base bias topology. The range of values at the base is somewhat limited because of the current mirror implementation, but it is sufficient for the desired operating region. The noise plot shows that the capacitor between the base nodes of the two transistors does add some noise to circuit, but it is far less than the base switch topology.

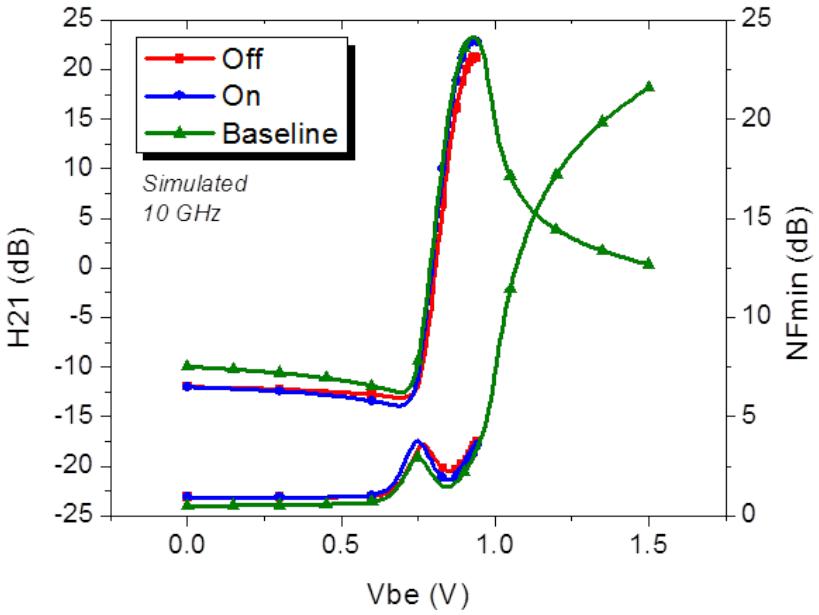

Figure 3.33: Resistive base bias topology H_{21} and NF_{min} over V_{be} at 10 GHz.

The Smith chart in Figure 3.34 shows that in this topology, switching in the additional core changes the imaginary part of S_{11}, S_{22}, and G_{min}. The change in the real part of the impedances is relatively small. This topology agrees well with the theory described previously.

The power handling of the resistive base bias architecture is much lower than the other topologies, as seen in Figure 3.35. This is due to the loading effect of the current mirror. To reduce this effect, other biasing topologies may be investigated. Even though the power handling is reduced, there is still significant improvement in P_{1dB} and gain from the off to on state.

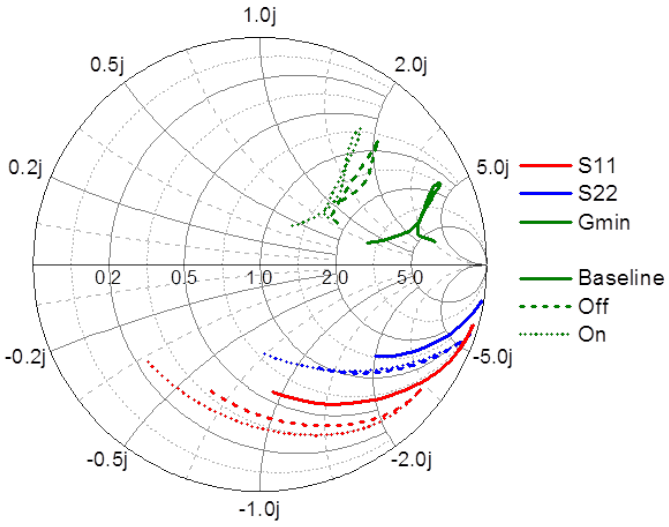

Figure 3.34: Base bias topology Smith chart at 10 GHz over V_{bias}.

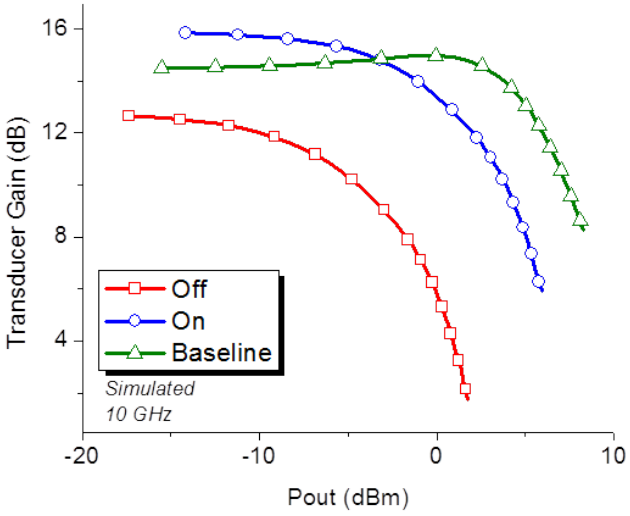

Figure 3.35: Base bias topology power handling at 10 GHz.

Another benefit of the resistive base biasing topology is that it can be tuned for a wide range of values. In the emitter and base switch topologies, there is only an on and off state. However in the resistive base biasing topology, the base voltage supplied by the current mirror can be varied so the additional transistor conducts a little current, a lot of current, or anywhere in between. This is very powerful and

can help tune the imaginary part of the input match or change center frequencies. Figure 3.36 shows the H_{21}, NF_{min}, and Smith chart as the bias voltage is varied. The H_{21} indicates the gain may be selected through the bias voltage of the second current mirror while maintaining a reasonable noise figure. The Smith chart shows that the bias voltage of the second current mirror can change the imaginary part of the S_{11}, S_{22}, and G_{min}, while the real part remains relatively unaffected. In this way, the resistive bias topology can be used to tune the imaginary part of the input match.

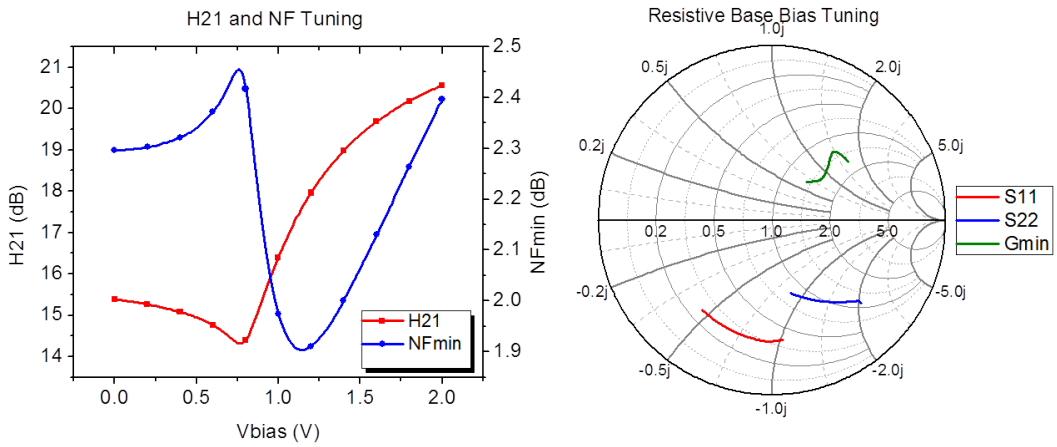

Figure 3.36: Tuning of the base bias topology at 10 GHz over V_{bias}.

3.4 Reconfigurable LNA

The resistive base bias topology was investigated further and applied to a cascode LNA design. This topology is especially appealing because it provides continuous tuning capabilities rather than a set of discrete states. Figure 3.37 shows the schematic of the switchable core cascode LNA. When zero volts is applied to V_{bias2}, the voltage at the base of Q3 is also force to zero and no current flows through Q3 and Q4. When the bias voltage is increased, the second cascode pair provides another path to amplify the RF signal. This improves the power handling capabilities and may even be used change the center frequency of the input match.

The design process of the switchable cascode LNA is similar to the narrowband

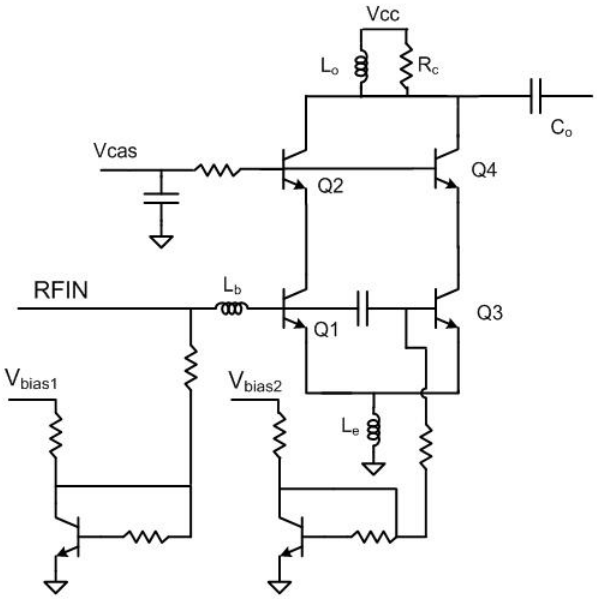

Figure 3.37: Schematic of the reconfigurable LNA.

LNA. Once again the simultaneous power and noise match approach described in [34] is utilized to determine the values of the base and emitter inductors. The transistors in this design were biased at the same current density as that of the narrowband design for comparison purposes. Each transistor was chosen to have the largest emitter length of 10.16 μm to achieve a wide tuning range. The simulated S-parameters when the second cascode pair is turned off are seen in Figure 3.38.

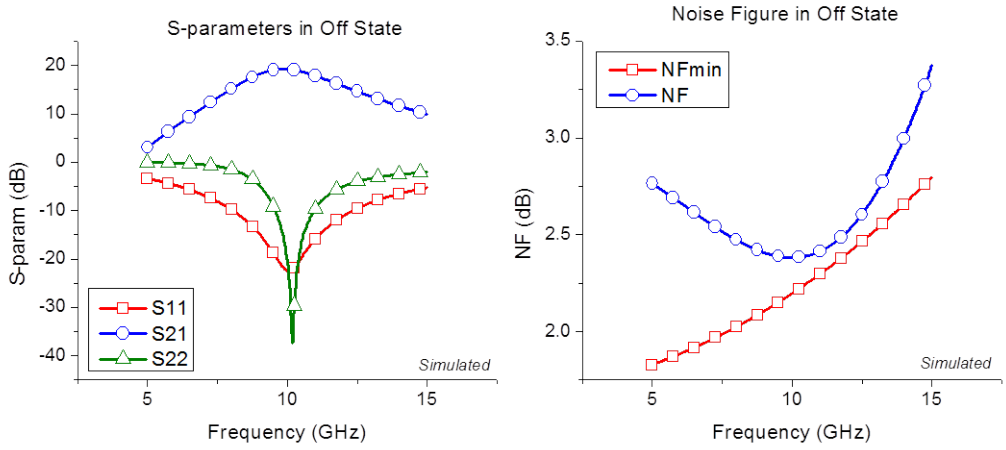

Figure 3.38: S-parameters and noise of the reconfigurable LNA in the off state.

As expected from the transistor core simulations, switching in the second cascode pair enables tuning of the input center frequency while maintaining a good match to 50 Ω. The addition of the matching inductors (L_b and L_e) degenerates the effect of adding the second transistor core and results in a reduced tuning range. However, a tuning range of over 1.7 GHz is still achieved with a return loss of less than 25 dB at the center frequency. Figure 3.39 shows the S_{11} of the LNA at several bias points and the center frequency as a function of the bias voltage. For these simulations, the first transistor is set to the desired current density, while the bias of the second transistor is swept

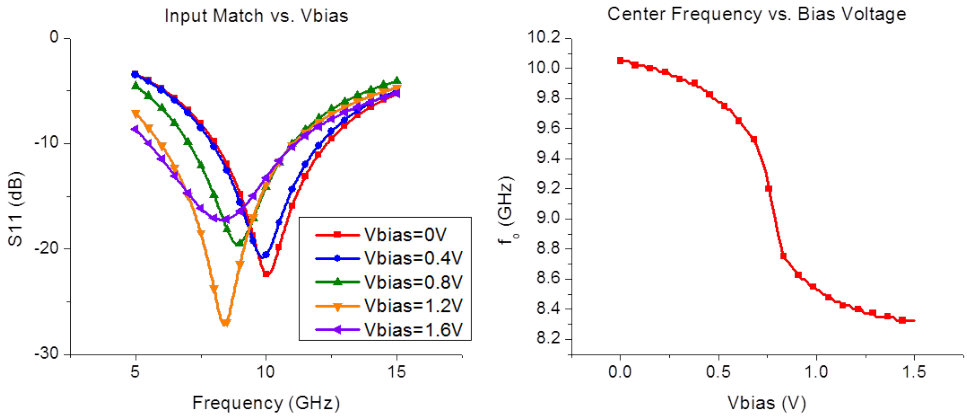

Figure 3.39: Center frequency as a function of V_{bias2}.

The effect of adding the switchable core on the noise figure is more complex to analyze. In this design, two 10.16 μm transistors are used to achieve a wide tuning range. This sizing causes the real part of the optimum noise match to be more than 50 Ω. As a result, adding a second transistor in parallel to the first device reduces the optimum noise impedance towards 50 Ω and improves the noise figure. Figure 3.40 shows the noise figure at 10 GHz as a function of the voltage applied to V_{bias2}.

Figure 3.40 shows the noise increases at high voltage biases. However, the voltage bias effectively changes the center frequency. Thus, the noise does increase at 10 GHz, but this is not necessarily the operating frequency for all bias voltages. It is more

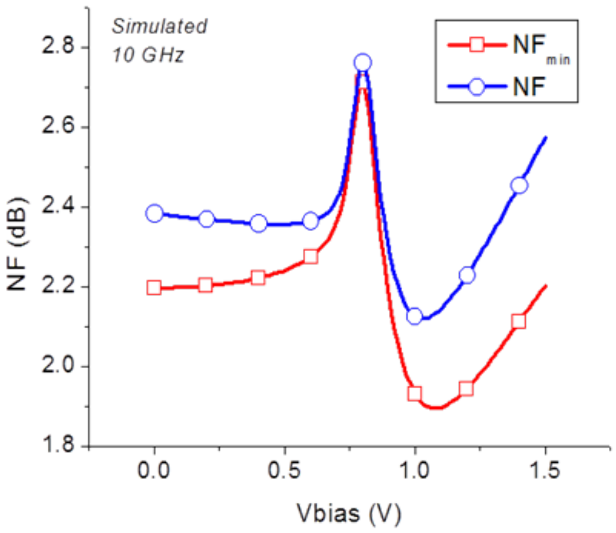

Figure 3.40: Noise figure at 10 GHz as a function of V_{bias2}.

informative to look at the noise figure at the center frequency for each bias point. Figure 3.41 shows the noise figure as a function of the center frequency. This graph shows two local minimum points in the noise figure curve. These points correspond to the biases where the transistors are operating at ideal current densities for low noise figure. The first transistor is initially biased to a current density with low noise figure so with the second transistor turned off, a good noise figure is achieved. With the second transistor at low biases, the small current density through the second device results in a large noise figure. When the second transistor reaches the ideal current density for minimum noise figure, the second local minimum is reached. To reduce the frequency spacing between local minimums, several small transistor cores could be used instead of two large transistors. The noise figure of the LNA is degraded some from the simple narrowband case, but it is still less than 2.6 dB from 8.3 GHz to 10 GHz. This is an acceptable trade off for some applications.

Harmonic balance simulations show the full LNA design agrees well with the earlier predictions from simulating the transistor core. Figure 3.42 shows that the bias

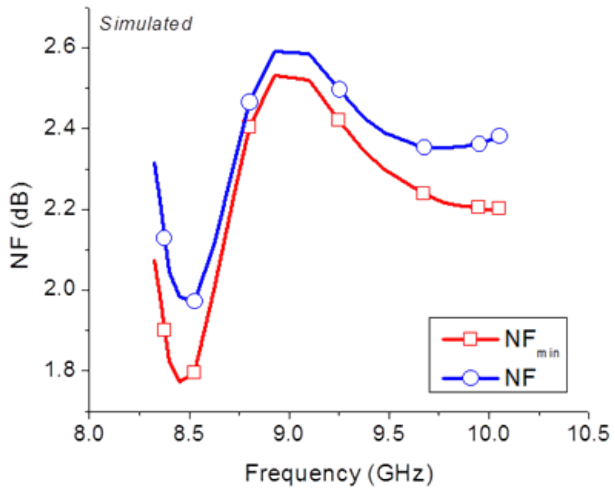

Figure 3.41: Noise figure at the center frequency.

voltage for the second current mirror can be used to tune the gain and P_{1dB}. At low voltage biases, before the second transistor is turned on, there is little change to the gain and P_{1dB}. As the voltage is increased above the threshold voltage, the transistor begins to conduct significant current, and the gain and P_{1dB} start to increase.

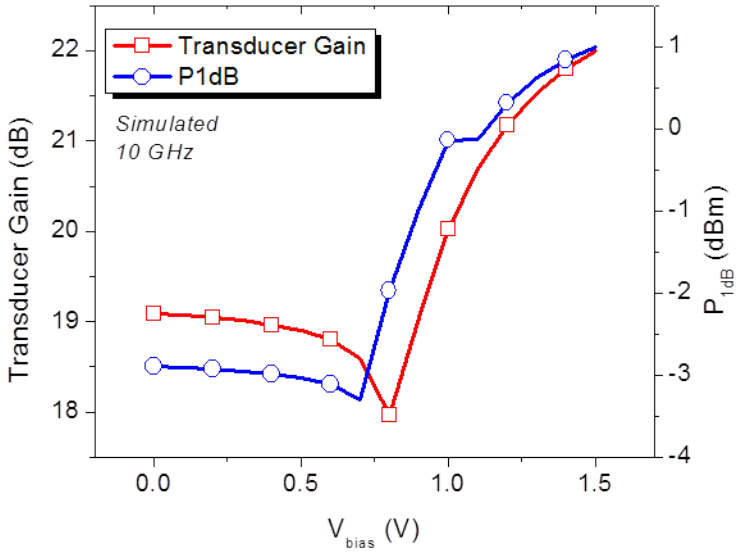

Figure 3.42: Gain and P_{1dB} as a function of V_{bias2}.

The LNA presented offers many attractive qualities for reconfigurable radar designs. First, it doesn't require a large number of tunable passive networks at the input, which can lead to losses and increased noise figure. In addition, it rejects signals out of the band of interest and prevents undesired noise from coupling into the signal. Finally, it offers tuning capabilities and is not just a set of discrete states. The next step is to transition this design to layout. As parasisitcs are included, a thorough stability analysis as outlined in the previous section will be conducted to ensure proper operation.

Research will continue to further explore and compare all the switchable core topologies. While the switchable cores change the input matching network, a tunable output network will also have to be implemented. The use of multiple switchable cores will be investigated for finer tuning and more flexibility. Eventually, a more complex design combining several different switchable core architectures may be designed to offer even further flexibility. Transistor core simulations show the resistive bias topology changes the imaginary part of the input match, and the emitter switch topology changes the real part of the input match. These topologies could be combined as shown in Figure 3.43 to create an LNA where the real and imaginary parts of the input match are independently tunable. This type of control and flexibility could enable a high performance reconfigurable radar system.

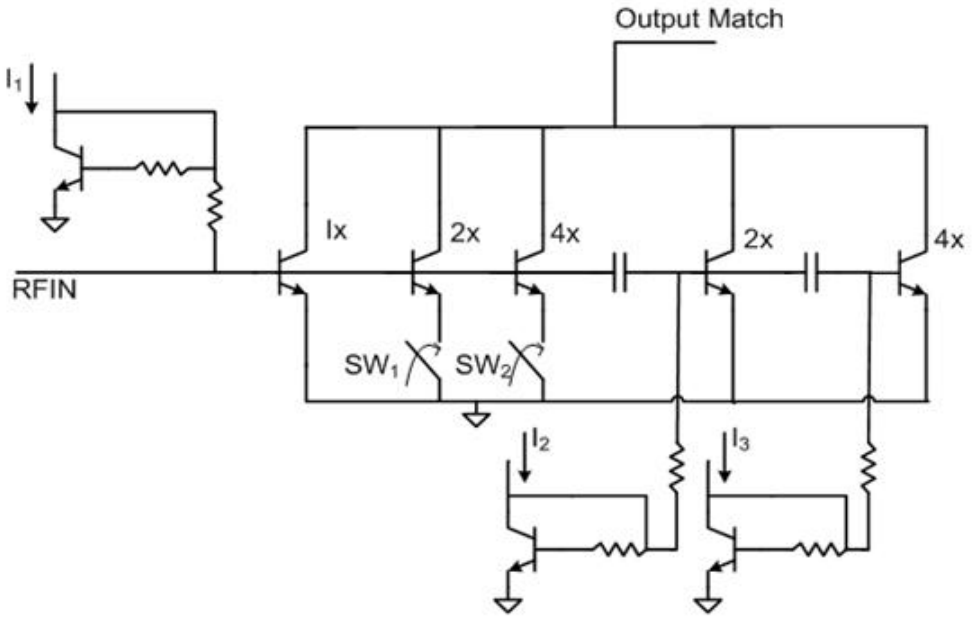

Figure 3.43: Schematic of a complex reconfigurable LNA.

CHAPTER IV

DESERIALIZER

Developing a reconfigurable system adds flexibility, but it is also more complex and requires many digital control signals. While separately biasing each control signal is manageable for a single die, it becomes unwieldy for a phased-array radar system. If a simple TRM requires six control bits and eight of these modules are used to form a phased-array radar system, then the system requires nearly 50 separate control signals. One way to reduce the number of control signals and make the system more manageable is to use a deserializer (serial-to-parallel converter).

A deserializer is a simple digital block that converts a serial data stream into many separate control signals. Typically, a deserializer block includes reset, clock, data, and latch inputs. Although some deserializers have more complex decoding functionality to improve reliability, a simple deserializer is essentially a first-in-first-out buffer in which the shift register (SR) values are held after a pulse on the latch signal. A conceptual diagram of the deserializer is shown in Figure 4.1.

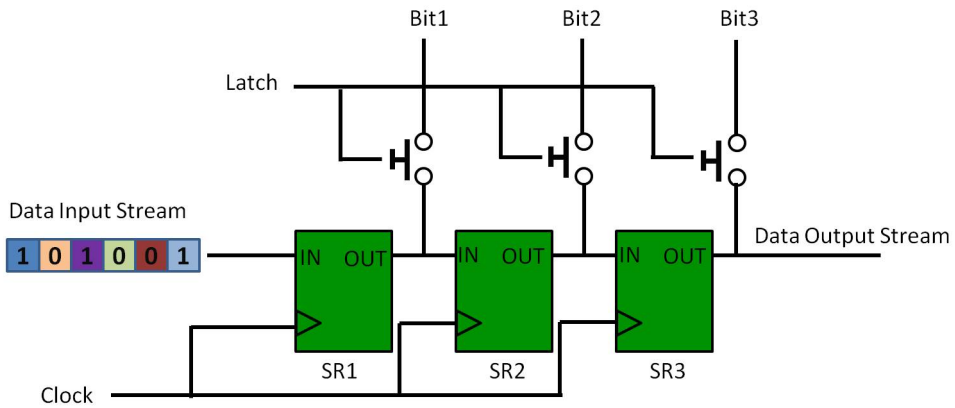

Figure 4.1: Simple deserializer diagram.

The reset, clock, data, and latch signals can be generated off chip using an FPGA. This allows for a large number of control bits to be set while only requiring four inputs. There are additional benefits to using a deserializer when several chips are combined into a phased-array system. If the separate TRMs are in close proximity to one another or on the same packaging material, the reset, clock, data, and latch signals can be cascaded from one TRM to the next. Figure 4.2 shows an example where the deserializer is used with several cascaded TRMs. In this case, when the buffer in the first TRM is full, it pushes data onto the next TRM. Once the data stream fills the shift registers of all the array elements, the control signals are latched to the correct values. With this technique, the phased-array system of eight TRMs with six control bits each only requires four inputs; reset, clock, data, and latch. While this greatly reduces the complexity of the system, it does have some drawbacks. If one element in the chain fails, all elements after it will not function properly. For this reason, it is not appropriate to use this technique for very large systems.

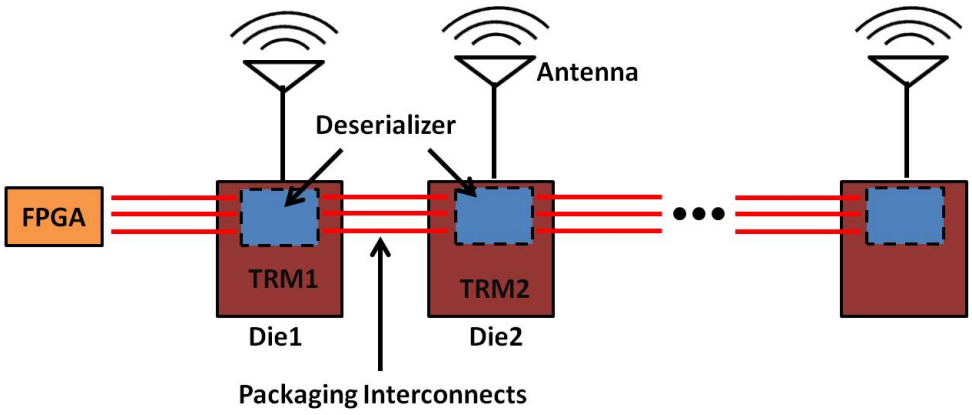

Figure 4.2: Cascaded deserializers in a phased-array system.

4.1 Digital Design Flow

The timing of signals is critical to the design of digital blocks like the deserializer. While digital logic can be created by combining simple primitive blocks (AND, OR,

etc), ensuring the correct timing becomes very challenging as the logic becomes more complex. Several tools have been developed to help designers meet timing requirements and verify design functionality. Figure 4.3, illustrates the design flow used to create the deserializer block.

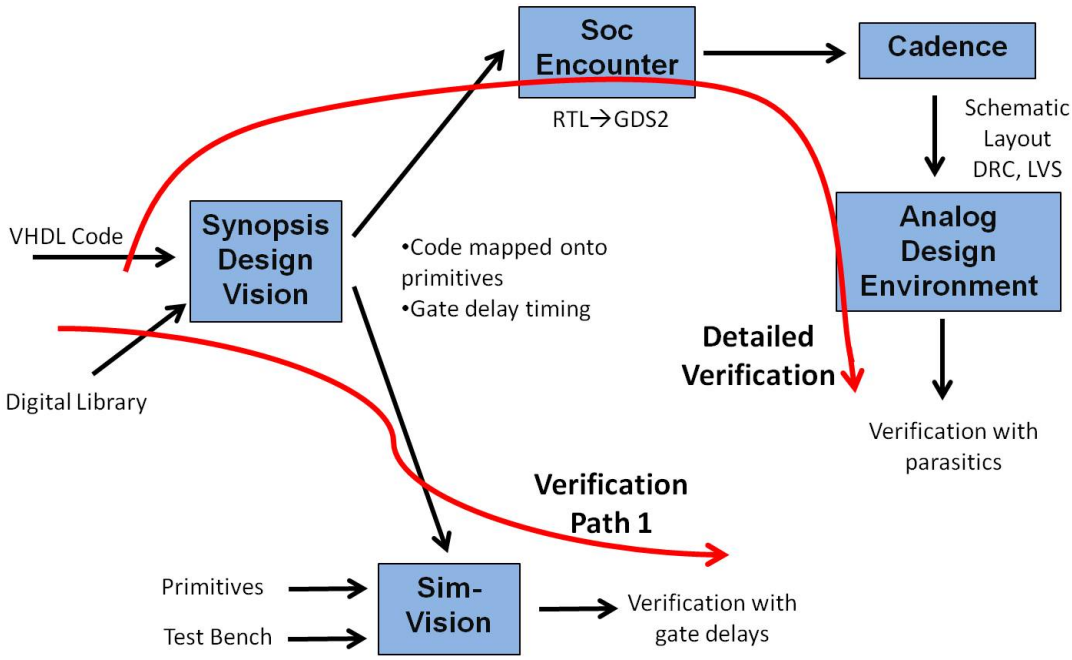

Figure 4.3: Digital design flow.

First, the deserializer functionality is written in VHSIC hardware description language (VHDL) and verified in simulation. The VHDL deserializer code is fed into Synopsis Design Vision. After specifying timing constraints and signal loading, this program converts the high level hardware description language into a set of primitive blocks (AND, OR, etc). The logic of the netlist generated by Design Vision is the same as the original VHDL code, but it only uses the primitive components available in the specified design kit. The logic of this netlist is verified in Sim-Vision using a Verilog test bench to create the input signals. To make simulations more accurate, the gate delays associated with the primitive blocks are back annotated to the circuit netlist. While including gate delays improves the accuracy of the simulation, it does not include any information on the delays from interconnect lengths and parasitics.

Soc Encounter converts the netlist of primitive cells into a physical layout. The schematic and layout are imported into Cadence where the cell is checked to ensure it passes all design rules and the layout matches the schematic. A parasitic extraction tool within Cadence is used to determine the parasitics due to interconnects and coupling. The design is then resimulated including these parasitics to verify the interconnects do not change the digital functionality. Figure 4.4 shows the final layout of a 3-bit deserializer created to set the bits of a phase shifter in a phased-array radar system. The final layout including power and ground rings is 60 μm x 80 μm. In simulation, the deserializer block functions properly at speeds up to 400 MHz. This was more than sufficient for the desired application.

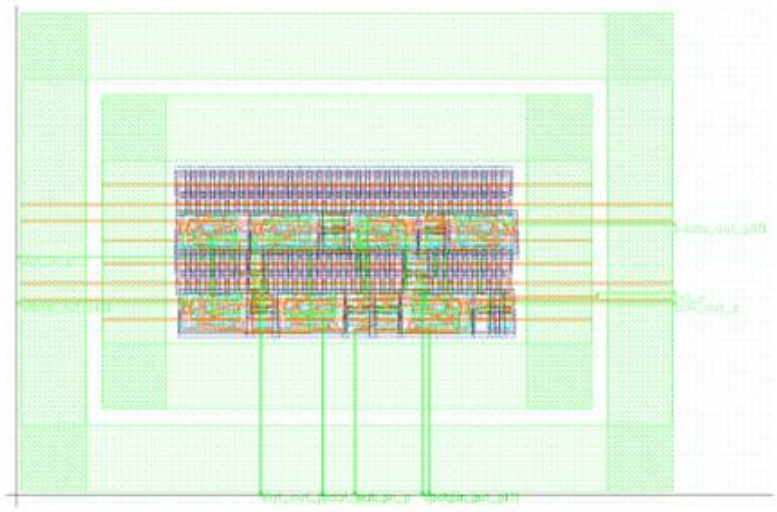

Figure 4.4: Final layout of the deserializer block.

4.2 Measured Results

After fabrication, the deserializer was wire bonded onto a Liquid Crystal Polymer (LCP) package for testing and integration. The reset, data, latch and a 100 MHz clock were provided by an FPGA. A MATLAB graphical user interface provide simple control over the input data stream. Figure 4.5, shows the input and output data streams of the deserializer measured on an oscilloscope.

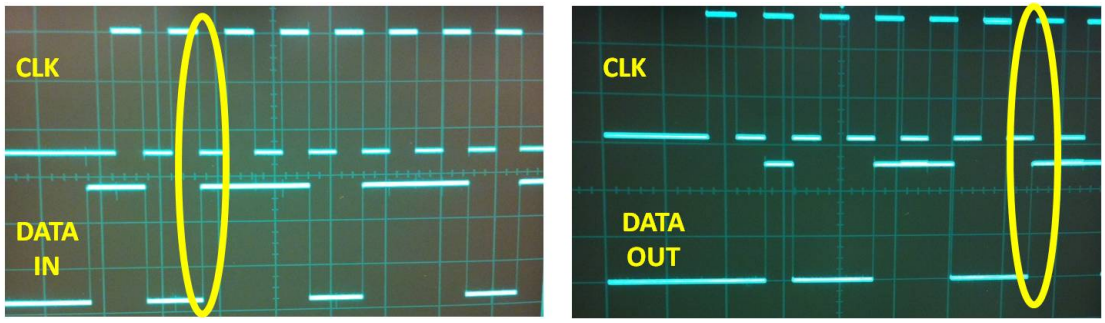

Figure 4.5: Measured deserializer input and output data streams.

The output data stream appears slightly distorted from the input stream. Theoretically, the output stream and input stream should be the same with a slight time delay. On the input side, the data stream is changing on the negative edge of the clock pulse. This gives the signal plenty of time to settle down before all the shift registers change on the rising edge of the clock. On the output stream however, the data stream is changing right before the positive clock edge. This creates problems for other deserializers down the chain since the data signal may not settle to the correct value by the time the register values are latched in. As a result, the correct output bits were observed for the first chip in the chain, but were distorted in the subsequent TRM modules. This problem can be easily fixed by changing the VHDL code so the output data stream changes on the negative clock edge.

Unfortunately, additional noise sources were not included in simulation so the deserializer still simulated properly. It was only after fabrication when real world noise and parasitics came in to play that the problem manifested itself. In addition to the change in the VHDL code, several improvements could be made to increase the reliability of this digital block. First, large buffers could be included on the output signals to increase the drive of the signal and reduce the rise and fall times. In addition, the inputs could use Schmitt Triggers to add hysteresis and reduce the sensitivity to noise [2]. These changes would make the deserializer more robust to factors not completely captured in simulation.

CHAPTER V

CONCLUSION

This work has described a unique approach of turning on and off transistor cores to reconfigure low-noise amplifiers. A small footprint single-pole, single-throw switch was optimized for low insertion loss and high isolation. A narrowband (non-switchable) LNA was developed as a basis of comparison for reconfigurable designs. The optimized switch was incorporated into different switchable transistor core architectures. These architectures were investigated to determine their ability to reconfigure amplifier performance. One switchable transistor core topology was integrated into a cascode LNA design. An in depth stability analysis using the S-probe technique helped improve the reliability of the cascode design. In addition, a single-pole, double-throw transmit/receive switch, as well as a deserializer were developed to help support the LNA block in a reconfigurable phased-array radar system. This type of flexible radar design would be very attractive in challenging electromagnetic environments.

5.1 Future Work

The results of this research have raised many questions that will continue to be investigated. First, all the transistor core topologies will be further explored and transitioned to layout. The layout of these designs will be very challenging since the RF path must be split to drive the different transistor cores and then recombined at the output. Incorporating these transistor cores into LNAs or even power amplifiers (PAs) provides a multitude of possibilities to be explored. Further flexibility may also be achieved by combining switchable transistor cores with switchable passive networks and varactors. This work presented results where only a single transistor

was switched in and out. In the future, the limitations on how many switchable transistors can be combined will also be investigated. At some point the loading and losses associated with adding another transistor will outweigh the flexibility gained from turning the transistor on and off.

While the switchable LNA designed in this work focused on tuning the input match, the transistor cores can be used as control knobs to adapt to a variety of different environments such as temperature, spectral (jamming or interfering signals), and radiation. Further investigation of these control knobs could have a direct impact on mobile radar systems which frequently experience these different environments. In addition, reconfigurable designs will be pursued for the other building blocks in the phased-array system. The goal is to eventually combine these reconfigurable blocks into a highly controllable phased-array system and demonstrate its ability to adapt to different environments.

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